MKE304T
User Manual

Version: V1.2

Contents

Revision History

Version	Date	Major Changes
V1.0	2023-4-24	First release
V1.1	2023-5-17	1.Revised Rogowski coil sensor register description 2.Added description of error wiring registers
V1.2	2023-6-20	1.Modify the HSDC section description 2.Added a description of SAR registers to the ECT section 3.The EMUIF register attribute is revised to R/W 4.Revised description of relationships when HFCONST cascade is used

1.General Description

The MKE304T is a multi-functional, high accuracy, high-reliability, low consumption energy metering device, which can be widely used in smart meters, energy consumption analysis, power monitoring, power safety and other fields of meter design.

The MKE304T supports current transformers, shunt and Rogowski coil sensor, typical applications include: Power Grid Smart Meter (current transformer, shunt), Power Grid IoT meter (current transformer, shunt), Power Grid Guide Rail meter (Rogowski coil sensor).

This manual mainly introduces the system functions, register definitions, calibration methods and communication interfaces of polyphase energy metering device. Pin configuration and other model information, please refer to the *Polyphase Energy Metering IC Data Sheet*.

1.1.Functional Block Diagram
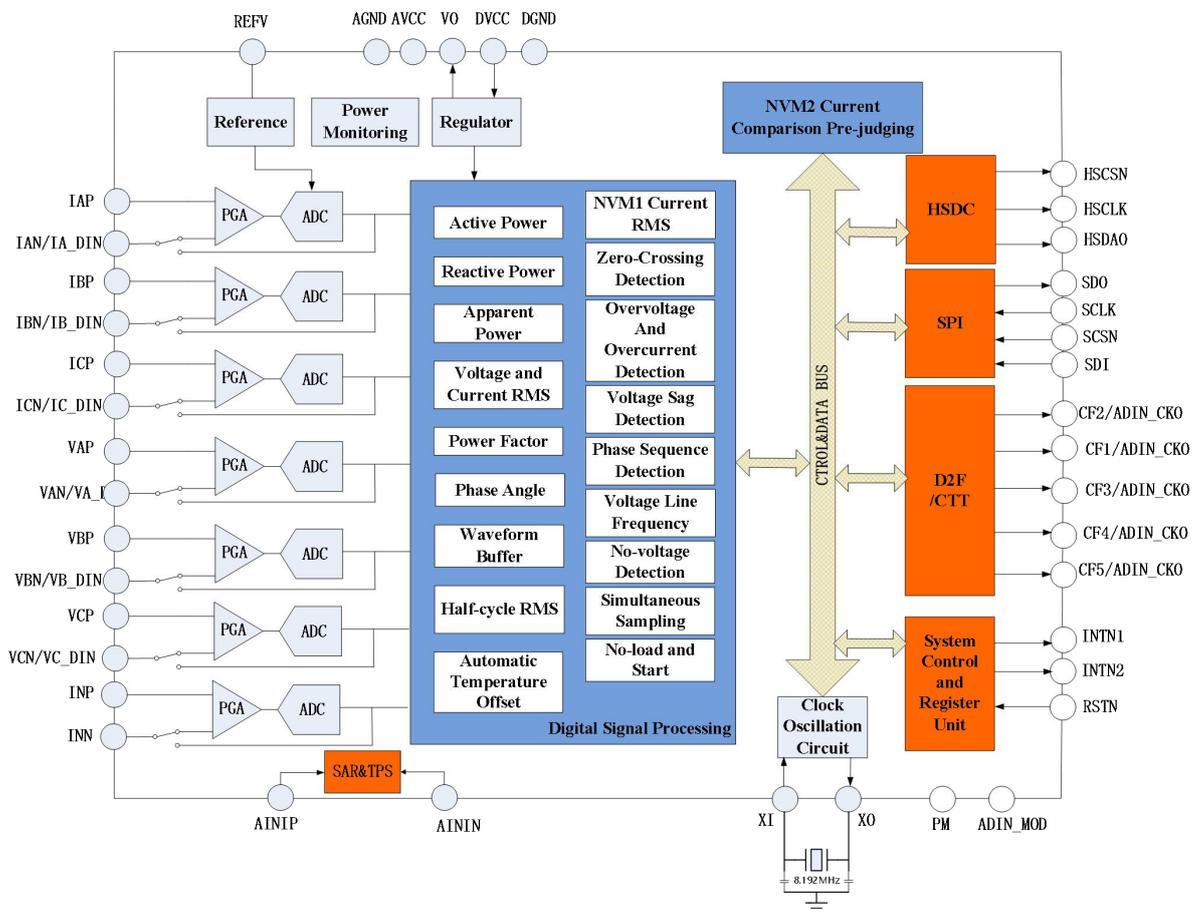
Figure 1-1 Functional Block Diagram

2.System Function

2.1.Operating Mode

The MKE304T is equipped with four operating modes, such as the energy measurement mode (EMM), **no-voltage** mode 1 (NVM1), no-voltage mode 2 (NVM2) and sleep mode (SLM).

●Energy Measurement Mode (EMM): It is used to measure and meter various electrical parameters when the energy meter operates in the power supply mode.

●External ADC metrology mode (ADCIN) is used to measure and meter each power parameter when the three-phase shunt meter is working in the power grid

●No-voltage Mode 1 (NVM1): It is used to measure the low power no-voltage current RMS.

●No-voltage Mode 2 (NVM2): It is used to pre-judge the low power no-voltage current.

●Sleep Mode (SLM): Use in the sleep status when the energy meter is powered by the backup battery after the power grid is powered down.

The operating mode switching is performed through the SPI command, and the mode switching command registers and command words are described in Section 3.5.

The effects and changes of mode switching on registers are described in Section 3.5.4. The system status register SYSSR (B1 0x8A) WMS [1:0] register bits indicate the chip's current operating mode.

After power-on and reset, the system default mode can be configured as SLM or EMM by the PM pin. The PM bit of the system status register SYSSR (B1 0x8A) register indicates the chip's current PM pin configuration.

The SYSSR (B1 0x8A) register is described in Section 3.4.42.

2.2.System Reset

The device supports the following reset modes:

● Power-up / Power-down reset

● External pin reset

● Software reset

● Wake-up reset

The power-up / power-down reset is the global reset, and other reset modes are the local reset. Upon completion of the reset, the reset flag bit of the system status register SYSR (B1 0x8A) changes. The reset flag bit is specified in Section 3.4.42 of the register.

1. Power-up / Power-down Reset

After the power-up / power-down reset has occurred, the system is reset to the default mode SLM or EMM that is configured by the PM pin. The register is reset to the initial value in the default operating mode. The external pin level is reset to the initial state. For the details on the power-up / power-down reset register, refer to Section 3.5.1.

2. External Pin Reset

When the system is in the SLM mode, the external pin reset is invalid. When the system is in the EMM, NVM1 and NVM2 mode, the external pin reset is valid. After the external pin reset has occurred, the current operating mode of the system is constant, and only part of registers are reset to the initial value in this operating mode. For the details on the external pin reset register, refer to Section 3.5.2.

3. Software Reset

For the details on the software reset command registers, refer to Section 3.4.33.When the system is in the SLM mode, the software reset is invalid. When the system is in the EMM, NVM1 and NVM2 mode, the software

reset is valid. After the software reset has occurred, the current operating mode of the system is constant, and only part of registers are reset to the initial value in this operating mode. For the details on the external pin reset to register, refer to Section 3.5.3.

4. Wake-up Reset

When SLM or NVM2 is switched to EMM or NVM1, the wake-up reset takes place. After the reset has occurred for 1.5ms, the register is reset to the initial value of the wake-up reset. For the details on the wake-up reset register, refer to Section 3.5.4.

2.3. Power Supply Monitoring

The chip contains an on-chip 3.3V analog supply monitor supervises the supply AVCC. When AVCC is lower than 2.70V under the room temperature, the MKE304T is reset globally. When AVCC is higher than 2.82V under the room temperature, the MKE304T operates normally.

2.4. Measurement Mode

The measurement mode is used to realize the measurement and metering function of each power parameter when the meter works in the power grid.

Support two measurement operating modes: EMM mode and ADCIN mode.

The EMM mode sampling channel includes seven ADCs and their sampling data processing circuit.

In ADCIN mode, the seven sampling channels can be configured as internal ADCs or external ADCs. However, in the application of polyphase shunt meter, there are generally the following two configuration schemes:

Scheme 1: the sampling channel includes three external ADC inputs of current channels, one internal current channel ADC and three internal voltage channel ADCs;

Scheme 2: The sampling channel includes seven external ADC inputs and their sampling data processing circuits. The chip can enter ADCIN mode by configuring the software and hardware or just the software.

2.4.1. Sampling Channel

- In EMM mode, sampling channels include seven internal Σ-ΔADCs, where IA/IB/IC is used for phase line current sampling, IN is used for null line current sampling, and U/UB/UC is used for voltage sampling.

- In ADCIN mode, the seven sampling channels can be configured as internal ADCs or external ADCs. However, in the application of polyphase shunt meters, there are generally the following two configuration schemes.

  - Scheme 1: Use four single-phase ADC chips. Three of them are used for phase line current sampling and one is used for null line current sampling; the external input clock required by the ADC chip is output from the ADIN_CKO pin of the chip to ensure that the clocks of the two chips are of the same origin; the sampling output of the ADC chip is input from the IA_DIN, IB_DIN, IC_DIN, and IN_DIN pins of the chip.

  - Scheme 2: Use four polyphase shunt meter ADC chips . Three of them are used for both voltage and current sampling, and the other is used for null line current sampling. The external clock required by the ADC chip is output from the ADIN_CKO pin of the chip to ensure that the clocks of the two chips are of the same origin; The ADC chips sampling output of the ADC chip is input from the chip's IA_DIN, UA_DIN, IB_DIN, UB_DIN, IC_DIN, UC_DIN, and IN_DIN pins.

The internal Σ-Δ ADC is used for voltage sampling, totaly differential input, the maximum differential signal input amplitude peak is 830mV. The internal ADC can be configured with PGA amplification of 1/2/4/8 times by configuring the ADCCFG register (B1 0x83), and the internal ADC reference can be selected from the internal reference or an external reference. The use of ADCCFG registers is described in Section 3.4.5.3.

Register ADCIN_CFG (B1 0xA0) can be configured in ADCIN mode, and seven channels can be configured separately in ADCIN mode to select internal or external ADCs, ADCIN_CFG registers are described in Section 3.4.5.6.

By configuring the SYSCFG register (B1 0x78), the ADCxx_PD register bits can switch each ADC independently. The SYSCFG registers are described in Section 3.4.34.

The polyphase measurement module after the 1-bit flow in different modes and schemes above is exactly the same.

Seven sampling channel phase calibrations are enable by configuring the PHS registers (B1 0x0C-0x12), which are described in Sections 3.4.7 and Chapter 4 Calibration Method. Three current channel segment phase calibrations are enable by configuring the phase compensation region setting register PRTHx (B1 0x06-0x09), which is described in Section 3.4.5.

Seven sampling channel gain calibrations are enable by configuring the GS register (B1 0x13-0x19), which can be used in Sections 3.4.8 and Chapter 4 Calibration Method.

High pass filter of seven sampling channels are enable/disable by configuring the HPFOFF [6:0] register bits in the EMUCFG register (B1 0x61) for testing DC parameters. HPFOFF [6:0] is described in Register Sction 3.4.18.1.

The value of the DC_OS register (B1 0x1A-0x20) can be automatically calculated by configuring the AUTODC_EN register (B1 0x91) for seven sampling DC OFFSET calibration, AUTODC_EN register is described in Section 3.4.40 and DC_OS register is specified in Section 3.4.9.

The seven real-time sampling data are divided into total data and fundamental data, which can be output to the waveform sampling register, the sampling rate is fixed at 8KHz, and the data source is the data after the ADC has passed through the high-pass filter. The waveform sampling registers are described in Section 3.2.1.

2.4.2. Sampled Waveform Buffer

Seven 24bits sampling data can also be stored in the internal waveform memory unit for FFT analysis.

1. **Buffer Area Capacity**

The buffer area has a total of 896 address units, and can store up to seven ADC UA, UB, UC, IA, IB, IC, IN 128-point data one-cycle or 256-point half-cycle data or 512-point 1/4 cycle data.

2. **Address Mapping**

1) Byte Length: There are three bytes for one address unit, which is used to store one sampling data of ADC.

2) Address Mapping: 896 address units with the encoding address 200H-57FH.

3. **Sampling Rate and Buffer Control**

The chip offers two waveform sampling modes, fixed sample rate mode and simultaneous sampling mode, configured by the DMA_WAVECON (B1 0x93) register, the mode selection of which is shown in the figure below:
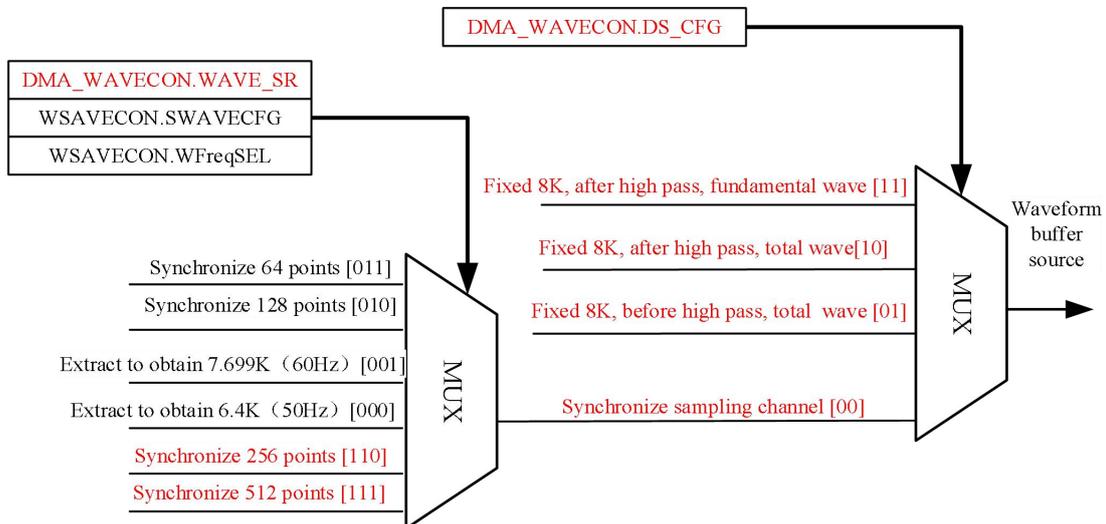
DMA_WAVECON.DS_CFG[1:0] perfoRMS waveform buffer source selection.

DMA_WAVECON.DS_CFG[1:0]=00 is selected as the simultaneous sampling mode, in which the sampling rate tracks the change of the fundamental sample frequency. By DMA_WAVECON. WAVE_SR, WSAVECON. SWAVECFG, WSAVECON. WFreqSEL three register bits selectable: fixed 64 points/cycle, fixed 128 points/cycle, fixed 256 points/cycle, fixed 512 points/cycle, 6.4KHz waveform sampling rate at 50Hz (fixed 128 points/cycle), 7.699K waveform sampling rate at 60Hz (fixed 128 points/cycle). Synchronous tracking power grid frequency range: 40~70Hz, can be used for FFT analysis and harmonic content calculation.

DMA_WAVECON.DS_CFG[1:0]≠00 is selected as a fixed sample rate mode, the waveform sampling rate in this mode is fixed at 8KHz, and the fixed sampling waveform data source is further selected by configuring the DS_CFG [1:0]:

DS_CFG[1:0]=01 is selected as the high-pass filter (HPF) before fixed 8KHz sample rate total data;

DS_CFG[1:0]=10 is selected as the high-pass filter (HPF) followed by fixed 8KHz sample rate total data;

DS_CFG[1:0]=11 is selected as the high-pass filter (HPF) and then fixed 8KHz sample rate fundamental data.

See Section 3.4.20 for details.

4. **Sampling Rate and Buffer Control**

Whether the ADC data of each channel is written to the buffer and the arrangement of the buffer area, the size of the buffer of each channel, the start-stop buffer, and the state of the buffer after the buffer action is started, are controlled by the sample data write buffer control register WSAVECON (B1 0x63), see Section 3.4.20 for details.

5. **SPI BURST Read Operation of Buffer**

Users can read the buffer data by SPI. For the details on the read operation of the buffer SPI, refer to Chapter 5 Communication Interface.

When SPI reads the waveform buffer successtotaly for one time, the data buffer addresses read for the last time are stored in the waveform buffer address register LRBufAddr (B1 0x8E). For the details on the LRBufAddr register, refer to Section 3.4.36.3.

6. **Operating Mode and Waveform Buffer:**

The waveform buffer in SLM, NVM2 and NVM1 is invalid. The waveform buffer RAM is uncertain in the EMM/ADCIN mode after the power-up reset or the wake-up reset, write the value after write buffer or clear command. For the software reset and the hardware pin reset, the waveform buffer RAM is constant.

2.4.3. Active Power

The chip has total/fundamental per-phase active power, all-phase active power, per-phase instantaneous power and per-phase half-cycle active power, and has per-phase/all-phase active power symbol bits for four-quadrant judgment, in addition to active power gain calibration, phase calibration and offset calibration registers.

1. Per-phase Active Power

For the details on the per-phase active power Px (x = A, B, C, the same below) register, refer to Section 3.2.3.
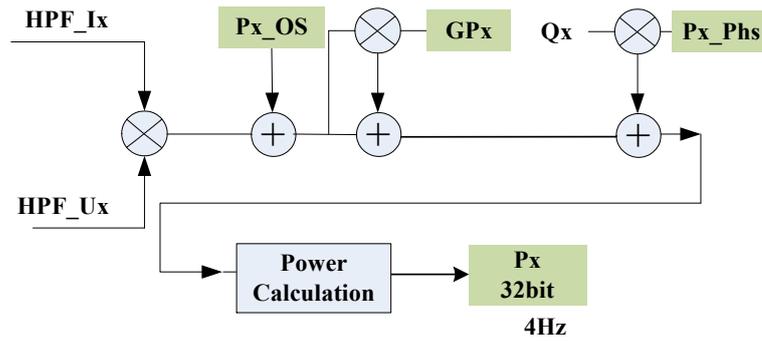
As shown in the figure, carry out the active power gain calibration by the register in the per-phase active power channel. For the details on the GPx register, refer to Section 3.4.11.

The active power phase is calibrated by the Px_PHS register in the per-phase active power channel. For the details on the Px_PHS register, refer to Section 3.4.12.

The active power Offset is calibrated by the Px_OS register in the per-phase active power channel. For the details on the Px_OS register, refer to Section 3.4.13.

2. All-phase Active Power

The average of the all-phase active power register P_T (B0 0x17) is the algebraic sum of the average active power for each per-phase. For the details on the P_T register, refer to Section 3.2.3.

P_T can be configured into the three-phase four-wire algorithm and the three-phase three-wire algorithm by selecting the register MODSEL (B1 0x86) in the three-phase four-wire and three-phase three-wire mode.

For the details on the MODSEL register, refer to Section 3.4.33.

If it is configured into the three-phase four-wire system, $P_T = P_A + P_B + P_C$.

If it is configured into the three-phase three-wire system, the phase B power not participated in calculation, so $P_T = P_A + P_C$.

3. Fundamental Active Power

There is a set of the active power parameters and calibration registers which correspond to the total active power, and the fundamental power shares the MODSEL register with the total. For the details on the fundamental active power and calibration register, refer to Section 3.2.3, 3.4.11 - 3.4.13. The fundamental filter can attenuate the harmonic power with the frequency 120Hz or higher.

4. Instantaneous Total and Fundamental active power

Supports instantaneous power with 8KHz rate update, including per-phase active power, per-phase reactive power, per-phase fundamental active power, per-phase fundamental reactive power.

5. Half-cycle active power

Support half-cycle active power calculation and measurement method, half-cycle active power registers are HW_Px (B3 00H~02H) and HW_FPx (B3 06H~08H); The update cycle of the half-cycle active power register is configurable through the HW_PNum register; The default of the HW_PNum register is 0, which means that the active power of the half-cycle update is calculated as the half-cycle 80-point accumulation average; The minimum HW_PNum register can be configured as 1, which means that the average calculation is calculated by the accumulation of half-cycle 1 point, and the maximum can be configured as 511, which means that the average calculation is calculated by the accumulation of half-cycle 511 points half power.

By configuring bit3 (P_HW_SEL) and bit30 (FP_HW_SEL) in EMUCFG2, the chip total-wave/fundamental wave active calculation method (integration mode) can be selected as the half-cycle metering method, at which time SPL_Px register (B0 B1H~B3H) and SPL_FPx register (B0 B7H~B9H) are multiplexed to half-cycle active power, and the register is half-cycle update active power.

6. Active Power Direction

The total and fundamental active power direction of the per-phase and all-phase is provided by the power direction register PQSign (0x66). For the details on the PQSign register, refer to Section 3.4.21.

2.4.4. Reactive Power

Provide the total and fundamental per-phase/all-phase reactive power and the sign bit of the per-phase/all-phase reactive power for the four quadrants judging. Furthermore, provide the reactive power gain calibration, phase calibration and Offset calibration register.

1. Per-phase Reactive Power

Per-phase reactive power Qx (x=A，B，C, the same below), refer to Section 3.2.3 for register descriptions.
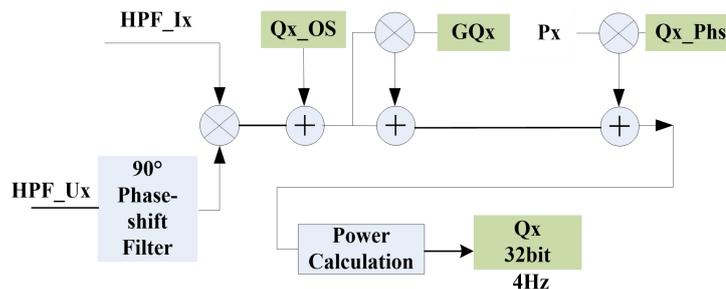
As shown in the figure, the active power gain is calibrated by the register in the per-phase reactive power channel. For the details on the GPx register, refer to Section 3.4.11.

In the per-phase reactive power channel, reactive power phase can be calibrate by Qx_PHS register, and the total reactive power phase calibration register supports phase segmentation calibration of the power channel, which can be used in conjunction with the phase compensation area setting register PRTHx. For the details on Qx_PHS register, refer to Section 3.4.12. The description of the phase compensation region setting register PRTHx is detailed in Section 3.4.5.

In the per-phase reactive power channel, the offset calibration of reactive power can also be performed by Qx_OS register. For the details on Qx_QS register, refer to Section 3.4.13.

The chip has a reactive 90° phase-shifted Hilbert algorithm, which can ensure good phase shift characteristics and amplitude-frequency response characteristics in the range of 0-51 harmonics.

2. All-phase Reactive Power

The average of the all-phase active power register Q_T (B0 0x1B) is the algebraic sum of the average active power for each per-phase. For the details on the Q_T register, refer to Chapter 3.2.3.

Q_T can be configured into the three-phase four-wire algorithm and the three-phase three-wire algorithm by selecting the register MODSEL (B1 0x86) in the three-phase four-wire and three-phase three-wire mode.

For the details on the MODSEL register, refer to Section 3.4.33.

In the three-phase four-wire system, $Q_T = Q_A + Q_B + Q_C$.

In the three-phase three-wire system, the power of phase B not participated calculation, so $Q_T = Q_A + Q_C$.

3. Fundamental Reactive Power

There is a set of the reactive power parameters and calibration registers which correspond to the fundamental reactive power, and the fundamental power shares the MODSEL register with the total reactive power. For the details on the fundamental reactive power and calibration register, refer to Section 3.2.3, 3.4.11 - 3.4.13. The fundamental filter can attenuate the harmonic power with the frequency 120Hz or higher.

4. Instantaneous Total and Fundamental Reactive Power

Supports instantaneous power with 8KHz rate update, including per-phase active power, per-phase reactive power, per-phase fundamental active power, per-phase fundamental reactive power.

5. Half-cycle reactive power

Support half-cycle reactive power calculation and measurement method, half-cycle reactive power multiplexing SQL_Qx register (Bank0 B4H~B6H) and SPL_FQx register (Bank0 BAH~BCH). If EMU_CFG2. P_HW_SEL = 1 (Bank1 9AH bit3), the register is updated half-cycle, and the register is half-cycle update reactive power. At the same time, the metering method is changed to the half-cycle metering mode.

Support half-cycle reactive power calculation and measurement mode, half-cycle reactive power registers are HW_Qx (B3 03H~05H) and HW_FQx (B3 09H~0BH); The update cycle of the half-cycle reactive power register is configurable through the HW_QNum register; The default of the HW_QNum register is 0, which means that the reactive power of the half-cycle update is calculated as the half-cycle 80-point accumulation average; The minimum HW_QNum register can be configured as 1, which means that the average calculation is calculated by the accumulation of half-cycle 1 point, and the maximum can be configured as 511, which means that the average calculation is calculated by the accumulation of half-cycle 511 points.

By configuring bit29 (Q_HW_SEL) and bit31 (FQ_HW_SEL) in EMUCFG2, the chip total /fundamental reactive calculation method (integration mode) can be selected as the half-cycle metering mode, at which time SPL_Qx register (B0 B4H~B6H) and SPL_FQx register (B0 BAH~BCH) are multiplexed to half-cycle active power, and the register is half-cycle update reactive power.

6. Reactive Power Direction

The total and fundamental reactive power direction of the per-phase and all-phase is provided by the power direction register PQSign (0x66). For the details on the PQSign register, refer to Section 3.4.21.

2.4.5.Apparent Power

Provide total/fundamental per-phase apparent power, and per-phase apparent power gain calibration registers. Provides total/fundamental RMS all-phase apparent power and PQS all-phase apparent power.

1. Per-Phase Apparent Power

The per-phase apparent power adopts the RMS method, namely, $Sx = U\mathrm{xrms}*I\mathrm{xrms}$, where UxRMS and IxRMS represent the RMS of x-phase.
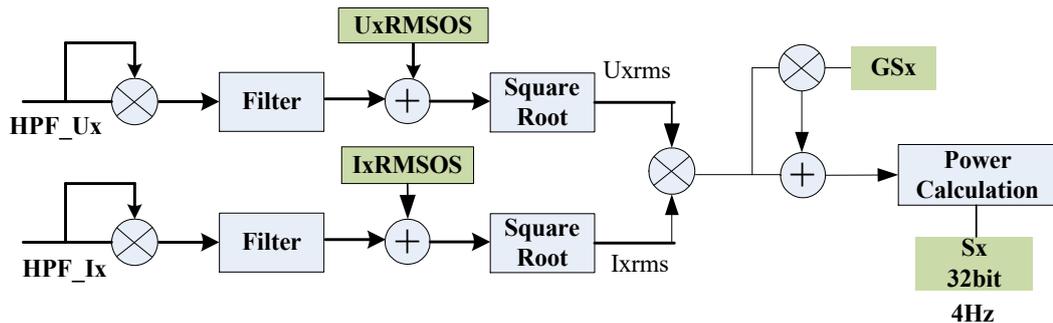
For the details on the apparent power register, refer to Section 3.2.3.

As shown in the figure, the channel gain calibration register GSU/I can calibrate the RMS gain and then calibrate the per-phase apparent power gain, and the channel gain calibration register GSU/I is detailed in Section 3.4.8; per-phase apparent power can also be calibrated by per-phase apparent power gain calibration register. For the details on per-phase apparent power gain calibration register, refer to Section 3.4.11.

2. All-Phase Apparent Power

Support two types of all-phase apparent power:

RMS all-phase apparent power: $S_{TA} = S_A + S_B + S_C$. This register is used under a three-phase four-wire and is not suitable for the three-phase three-wire case.

PQS all-phase apparent power: $S_{TV} = \sqrt{P_T^2 + Q_T^2}$, where P_T is all-phase active power, Q_T is all-phase reactive power.

The PQS all-phase apparent power can be configured in three-phase four-wire and three-phase three-wire mode through the MODSEL register, and P_T and Q_T are calculated according to the configuration of MODSEL register at this time.

3. Fundamental apparent power

There is a set of the apparent power parameters and calibration registers which correspond to the total apparent power, and the fundamental power shares the MODSEL register with the total. For the details on the fundamental apparent power and calibration register, refer to Section 3.2.3, 3.4.11 - 3.4.13. The fundamental filter can attenuate the harmonic power with the frequency 120Hz or higher.

2.4.6.Energy Output

Provide three energy output modes: energy register, CF frequency output and fast pulse count Fcnt.

1. Energy Register:

Provide several types of the energy registers, including the total/fundamental active/reactive/apparent, per-phase/all-phase and positive/reverse energy register. For the details, refer to Section 3.2.10 Energy Register.

2. Energy Pulse Output:

The all-phase pulse output, namely the Calibration Frequency output, can be connected with the standard energy meter for the error comparison directly.

Each CF output meets the following timing.
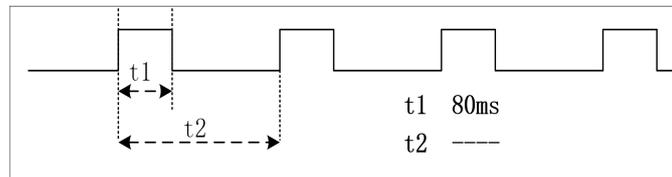
Note: When the pulse output period is less than 160ms, the pulse is output in the equal duty cycle way.

By default, CF1 is the all-phase pulse output of the total active power, CF2 is the all-phase pulse output of the total reactive power, CF3 is the all-phase pulse output of the total apparent power, and CF4 is the all-phase pulse output of the fundamental active power. Each CF pin can be configured into the any all-phase pulse output of the total all-phase active, total reactive, total RMS apparent, total PQS apparent, fundamental reactive, fundamental RMS apparent and fundamental PQS apparent power flexibly by the CFCFG register (B1 0x60) by default.

For the details of CFCFG register, refer to Section 3.4.17.

Each CF pin outputs the pulse by taking HFCONST1 as the high-frequency pulse constant, to synchronize the update of corresponding all-phase energy register by default. Each CF pin can take HFCONST2 as the high-frequency pulse constant to output the pulse by configuring the CFCFG register (0x60). At this time, if HFCONST1 is not equal to HFCONST2, the CF pulse output doesn't synchronize with corresponding all-phase energy register update. This function can be used for measuring the maximum demand pulse.

When the CF pin selects to use HFCONST2 to output pulses, select whether HFCONST2 and HFCONST1 are associated by configuring EMUCFG.HFCONST2_CFG. When this bit = 0, the two are not correlated, and if HFCONST1 is not equal to HFCONST2, the CF pulse output and the corresponding all-phase energy register update are not synchronized; When HFCONST2_CFG=1, HFCONST1 and HFCONST2 are used in series. When the pulse output is configured by HFCONST1, the pulse counter configured by HFCONST2 is incremented by one. Only when the counter value accumulates to the register of HFCONST2, the pulse configured by HFCONST2 is incremented by one.

Note: When HFCONST2_CFG=1, the pulse speed of the corresponding pin of HFONST1 is 2*HFCONST2 times of the output pulse speed of the corresponding pin of HFCONST2; For example, HFCONST2 should be configured to 0x5 when the output pulse speed of the corresponding pin of HFCONST1 is expected to be 10 times that of the corresponding pin of HFCONST2.

For the details of HFCONST register, refer to Section 3.4.1。

The MODSEL register is the three-phase four-wire mode by default. Accordingly, the all-phase pulse output of each CF pin is also the three-phase four-wire mode. When the MODSEL register is the three-phase three-wire mode, the all-phase pulse output of each CF pin is also the three-phase four-wire mode accordingly.

When the MODSEL register is the three-phase four-wire mode, configure the active all-phase energy cumulative mode in algebraic sum or absolute sum mode by configuring the EMUCFG.EPADDMOD0 register and the EMUCFG.EPADDMOD1 (BANK1 0X61) register. Accordingly, the all-phase pulse output cumulative mode of the active CF pin is also affected by the EPADDMOD0 register and the EPADDMOD1 register.

When the MODSEL register is the three-phase four-wire mode, configure the reactive all-phase energy cumulative in algebraic sum or absolute sum mode by configuring the EMUCFG.EPADDMOD0 register and the EMUCFG3.EPADDMOD1 (BANK1 0X6D) register. Accordingly, the all-phase pulse output cumulative mode of the reactive CF pin is also configured by the EPADDMOD0 register and the EPADDMOD1 register.

=2'b01 is an absolute sum mode, and the functional quantity of the all-phase is integrated with the absolute sum of the separated phase power | PA |+| PB |+| PC |;

=2'b10 is a positive accumulation mode, where the active energy of the all-phase is only accumulated in the positive direction of the separated phase power and integrated into the all-phase power;

=2'b11 is a negative accumulation mode, and the active energy of the all-phase is only accumulated into the all-phase power in the negative direction of the per phase power.

The default is algebraic sum mode.

The total/fundamental, active/reactive phase energy integration method selects algebra sum mode by default. By configuring EMUCFG2 (Bank1 0x9A), the per phase energy integration method can choose algebraic sum mode or absolute sum mode or positive accumulation mode or negative accumulation mode.

EMUCFG2.bit27~bit4 have a per-phase energy integration mode, taking phase A as an example:

=2'b01 is an absolute sum mode. In this mode, PAFCnt integrates | PA | and compares it with the corresponding HFConst. EPA increases by 1, and CF outputs pulses. In this mode, PAFCnt remains positive, EA=PosEPA, NegEPA=0;

=2'b10 is a positive accumulation mode, in which PAFCnt only integrates when PA $\geq$ 0. After comparing with the corresponding HFConst, EPA increases by 1, and CF outputs pulses. In this mode, PAFCnt remains positive, EA=PosEPA, and NegEPA represents negative active energy;

=2'b11 is a negative accumulation mode, which only integrates when PA<0. After comparing with the corresponding HFConst, EPA increases by 1 and CF outputs pulses. In this mode, PAFCnt remains negative, EA=NegEPA, and PosEPA represents positive active energy;

The default is algebraic sum mode, and each phase of active/reactive power for fundamental and total can be configured with separate modes.

For the details of EMUCFG (Bank1 0x61) register, refer to Section 3.4.18.1.

For the details of EMUCFG2 (Bank1 0x9A) register, refer to Section 3.4.18.2.

During the calibration process, if the user needs to output per-phase pulses, they can configure the measurement control register EMUCON (Bank1 0x60) to enable which phase participate in all-phase operations. If only required CF1 to output A-phase active pulse, PRUN0=1, PRUN1=0, PRUN2=0 in EMUCON can be configured, so B-phase and C-phase does not participate in phase energy calculation, and CF1 output pulse represents A-phase active pulse. For the details of EMUCON register (Bank1 0x60) , refer to Section 3.4.19.

3. Fast Pulse Count Register:

The fast pulse count register includes the total/fundamental active/reactive/apparent and per-phase/all-phase fast pulse count register. For the details, refer to Section 3.2.5.

4. Custom Power/HFCONST3/energy pulse output/energy register:

Provide 12 custom power and its corresponding energy registers, 3 custom CF pulse outputs CF6-CF8 and its companion HFCONST3 and HFCONST0/HFCONST1 for user use. Users can configure CFCFG1 register (bank2 0x9B) to configure CF6 as custom energy, A-phase total active, total reactive, total apparent, fundamental active, fundamental reactive, fundamental apparent in any kind of pulse output; CF7 is custom electric energy, B-phase total active, total reactive, total apparent, fundamental active, fundamental reactive power, fundamental apparent in any kind of pulse output, CF8 is custom electric energy, C phase total active, total reactive, total apparent presence, fundamental active, fundamental reactive power, fundamental apparent, fundamental apparent, any kind of pulse output in fundamental apparent. If custom energy is selected, the user can calculate the custom power from the ADC data or existing electrical parameters according to the needs and fill it in the custom power register. When you choose to configure the meter constant HFCONST3 after Custom Power, and configure HFCONST0/HFCONST1 after selecting HFCONST0/HFCONST1 after per-phase energy pulse, the chip will automatically integrate the output to the corresponding energy register and output the corresponding pulse CF6/CF7/CF8.

Before applying custom power registers D2FP00-11 and custom energy registers D2FE00-11, it is necessary to first configure D2FCFG [3:0]=4'b1001, address range Bank1 B0H~BBH registers as custom power registers D2FP00-11, and address range Bank1 BCH~C7H registers as custom energy registers D2FE00-11. When D2FCFG [3:0] is not equal to 4'b1001, the address Bank1 B0H~BBH registers are active and reactive segmented phase calibration registers, and the Bank1 BCH~C7H registers have no meaning.

The custom power register D2FP00~11 can be in twos complement format, 24 bits with signed numbers, of which the highest bit is the sign bit. When the value is written to the register, the power will be integrated according to the pulse constant HFCONST3, and the integrated electrical energy is stored in the D2FE00~D2FE11 register, of which D2FE00, D2FE01, D2FE02 can output pulses, corresponding pulses CF6, CF7, CF8 respectively; By default, the energy pulse CF6-CF8 cannot output the pulse waveform through the pin, and it is necessary to configure the D2FCFG [13:4] register to map CF6~CF8 to CF1~CF5 to output the pulse waveform.

Custom energy register D2FE00~11 is a 24bit register; It can be selected as cumulative mode or clear after reading mode, which is controlled by EMUCFG. ERegCAR (Bank1 0x61).

HFCONST3 can be used to configure meter constants, D2FE00~11 and CF5~CF7 share a HFCONST. In the same conditions, the value obtained according to the calculation formula of HFCONST1 multiplied by 4 can be used as the value of HFCONST3. The same meter constant energy output, the corresponding power register is correspondingly amplified by 4 times.

For the details of D2FCFG, D2FP00-11, D2FE00-11, HFCONST3 register, refer to Section 3.4.20.

The HFCONST0 register is 0 by default, and CF6~CF8 outputs pulses with HFCONST1 as the high-frequency pulse constant, synchronized with the corresponding energy register update. By configuring the HFCONST0 register (B1 0x5C) to be nonzero, the CF6-CF8 pin can be configured to output pulses with HFCONST0 as the high-frequency pulse constant.

2.4.7. Startup and No-load Setting

If a phase active power, reactive power or apparent power in a no-load status, the phase stops metering. FCnt register of this phase stops increasing, the phase energy register stops increasing, and the phase does not participate in the all-phase operation.

Support four startup and no-load mode:

● Fundamental current RMS startup mode

The RMS of the fundamental current of each phase is compared with the startup threshold register, and the startup and no-load criterion of total/fundamental and active/apparent/reactive energy of each phase is made.

● Total current RMS startup mode

The RMS of the total current of each phase is compared with the startup threshold register, and the active/apparent/reactive energy startup and no-load criterion of each phase is made, note that the fundamental current RMS and threshold comparison are still used in this mode

● Power startup mode 1

When the active power exceeds the threshold set by IStart_PS, the total/fundamental, active/apparent/reactive energy is activated; Or when the reactive power exceeds the threshold set by IStart_Q, the total/fundamental, active/apparent/reactive energy is activated.

● Power startup mode 2

Active, reactive, and apparent startup and no-load judgment is independent, and the startup threshold register is set separately for judgment. Comparison of active power and IStart_PS set threshold to make total/fundamental and active energy criteria. The comparison of reactive power and the threshold set by the IStart_Q is used as a total/fundamental reactive energy criterion. If either active or reactive power exceeds the threshold, the apparent electrical energy will be activated.

The four types of startup and no-load mode register configurations are as follows:

Startup and No-load Mode	EMUCFG3. Pstart_CFG[1:0]	EMUCFG.NoLoadCFG
Total current RMS startup mode	0x	0
Fundamental current RMS startup mode	0x	1
Power startup mode 1	10	x
Power startup mode 2	11	x

The description of EMUCFG3. Pstart_CFG and EMUCFG.NoLoadCFG register can refer to Section 3.4.18 and Section 3.4.18.1 respectively.

Provide two startup threshold registers IStart_ PS (Bank1 0x02) and IStart_ Q (Bank1 0x03), under the above four startup and no-load modes, IStart_ The scope of PS and IStartQ is shown in the table below:

Startup and No-load Mode	IStart_PS	IStart_Q
Total current RMS startup mode	Total active/apparent energy total current startup threshold, fundamental active/apparent energy fundamental current start-up threshold	Total reactive energy total current startup threshold, fundamental reactive energy fundamental current start-up threshold
Fundamental current RMS startup mode	Total/fundamental, active/apparent energy fundamental current startup threshold	Total/fundamental, reactive energy fundamental current startup threshold
Power startup mode 1	Total/fundamental, active/apparent/reactive energy active power startup threshold	Total/fundamental, active/apparent/reactive energy reactive power startup threshold
Power startup mode 2	Total/fundamental, active/apparent energy active power startup threshold	Total/fundamental, active/apparent energy reactive power startup threshold

The calculation formulas and usage instructions for IStart_PS and IStar_Q are detailed in Section 3.4.2.

Provide the startup and no-load judgment result register Noload (B1 0x67), which indicates the total active apparent/total reactive/fundamental active apparent/fundamental active apparent/fundamental reactive/fundamental apparent no-load state of each phase. For details on the no-load state register Noload, refer to Section 3.4.23.

2.4.8.Voltage RMS and Current RMS

For details on the RMS register, refer to Section 3.2.2.

1. Total Voltage RMS and Current RMS

The total Voltage RMS includes the polyphase Voltage RMS UA, UB and UC. The total current RMS includes the polyphase current RMS IA, IB, IC and the null current RMS IN.
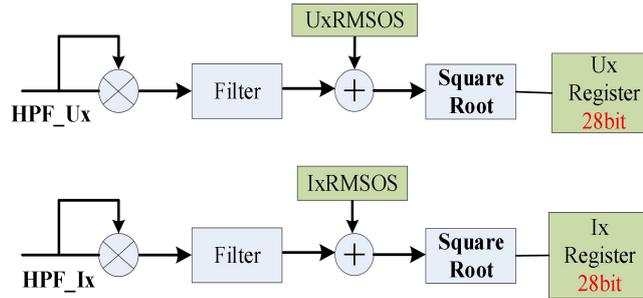
Figure 2-4 Voltage and Current RMS

Calibration of Voltage RMS and current RMS:

① Calibrate the gain by the channel gain register.

② RMS OFFSET calibration. For the details, refer to Section 3.4.7 and 3.4.8 and Chapter 4 Calibration.

2. Fundamental Voltage RMS and Current RMS

The fundamental Voltage RMS includes the polyphase fundamental Voltage RMS FUA, FUB and FUC; Fundamental current RMS includes the polyphase current RMS FIA, FIB and FIC and fundamental null RMS current FIN.

In addition to output as the parameters, FUA, FUB and FUC are also taken as the criterion for the voltage zero-crossing detection, voltage line frequency measurement and phase angle threshold detection. In addition to output as the parameters, the current RMS FIA, FIB and FIC are also taken as the criterion for the startup of each fundamental phases, current zero-crossing detection and current phase angle threshold detection. FIN shares the address with USUM or IN, and the value of USUM or IN can be configured through the EMUCFG3.FIN_SEL_IN (B1 0x6D) register bit to become FIN output.

Calibration of Fundamental Voltage RMS and current RMS: ① Calibrate the gain by the channel gain register.② Fundamental RMS OFFSET calibration. For the details, refer to Section 3.4.7 and 3.4.8 and Chapter 4 Calibration.

3. Harmonic Voltage RMS and Current RMS

The harmonic Voltage RMS includes the polyphase fundamental Voltage RMS HUA, HUB and HUC, and the harmonic current RMS includes the polyphase current RMS HIA, HIB and HIC.

The harmonic RMS can be used to calculate the harmonic content of voltage and current channel. The relationship among the harmonic Voltage RMS, total Voltage RMS and current RMS and fundamental Voltage RMS and current RMS is shown as follows:

$$HU_X = \sqrt{U_X{}^2 - FU_X{}^2} \; ; \; HI_X = \sqrt{I_X{}^2 - FI_X{}^2}$$

4. Voltage Vector sum RMS

It is defined as follows:

$$U_T = \frac{1}{4} * \sqrt{\frac{1}{T}\int_0^t (u_A(t) + u_B(t) + u_C(t))^2\, dt}$$

Where $u_A(t)$, $u_B(t)$ and $u_C(t)$ are the sampling of each voltage channel ADCs.

5. Current Vector sum RMS

There are two algorithms for the current vector sum current RMS, taking the three-phase four-wire system with the null current transformer and without the null current transformer into account.

Algorithm 1:
$$I_T = \frac{1}{4} * \sqrt{\frac{1}{T}\int_0^t (i_A(t) + i_B(t) + i_C(t))^2\, dt}$$

Algorithm 2:
$$I_T = \frac{1}{4} * \sqrt{\frac{1}{T}\int_0^t (i_A(t) + i_B(t) + i_C(t) - i_N(t))^2\, dt}$$

Where $i_A(t)$, $i_B(t)$, $i_C(t)$ and $i_N(t)$ are the sampling of various current channel ADCs.

Which algorithm is taken is depended by the ISUMMOD bit in the measurement unit configuration register EMUCFG (B1 0x61). If ISUMMOD=0, take the algorithm 1. If ISUMMOD=1, take the algorithm 2. For the details on the ISUMMOD bit, refer to Section 3.4.18.1.

The update cycle for above RMS data is 250ms.For the details on the RMS register, refer to Section 3.2.2.

2.4.9.Instantaneous Fundamental RMS

Provide instantaneous RMS SPL_FIA, SPL_FIB, SPL_FIC, SPL_FUA, SPL_FUB, and SPL_FUC with 8K rate updates.

2.4.10.Half-cycle RMS

Provide two sets of half-cycle RMS calculations, one of which is in the metering channel, starting from the zero-crossing point, and calculates the square of all points in the half-cycle and accumulates (or the arithmetic square root of the accumulation result); The other is in the synchronous sampling channel, using the same data source as the waveform buffer, which does not rely on zero crossing, and calculates the sum of squares of a fixed number of points and then squares.

2.4.9.1 Measurement Channel Half-cycle RMS

Half-cycle RMS registers UA_HW, UB_HW, UC_HW, IA_HW, IB_HW, IC_HW (B0 0xA0~0xA5), and IN_HW (B0 0xA9) are provided, and detailed in Section 3.2.3.

Definition: Starting from the zero-crossing point, the root mean square of the sum of the squares of all points in the half-cycle.

Calculation method: Half-cycle RMS register provides the sum of squares of the sampling points in the half-cycle. The user software does the root mean square operation.

Take phase A voltage as an example:

UA_HW=K_UAhw*sqrt(reg (UA_HW))

Where UA_HW is phase A voltage half-cycle RMS; reg (UA_HW) is the UA half-cycle RMS register after GSUA register gain calibration, and the gain calibration process can reuse the A-phase voltage RMS; sqrt is a square root operation that can be completed by software or configured as a chip; K_ UAhw is the conversion coefficient, which converts the test value into an indication value and is completed by the software.

- Performance:

  ◆ Voltage: Refer to power quality standards, S-level: 10%~150%Un, error<0.5%;

  ◆ Current: 5%In~Imax, error<0.5%; 1%In~5%In, error<2%

- Register update cycle: 100Hz (50HZ application)/120Hz (60HZ application).

- Applicable frequency: 50HZ/60HZ. The power grid frequency is selected through the EMUCFG.FreqSEL (50Hz/60Hz selection) register bit.

- Calibration method: gain calibration multiplexes RMS GSU/I register gain calibration process, and the conversion coefficient is completed by the MCU.

- Related registers: Channel gain registers GSU/I, EMUCFG.FREQ_SEL (B1 0x61) (50hz/60hz selection).

2.4.9.2 Simultaneous Sampling Channel Half-cycle RMS 2

Using the same source as the simultaneous sampling channel waveform buffer data, without relying on zero-crossing. The software configuration starts, calculates the sum of squares of fixed points and then calculates the square root, which is equivalent to implementing this formula: $\sqrt{\sum_{n=0}^{N} WAV_n^2}$, where N is any integer between 0 and 511, and WAVn is the instantaneous sampling of the nth point

2.4.9.2.1   Features

- Same source as simultaneous sampling channel waveform buffer data;
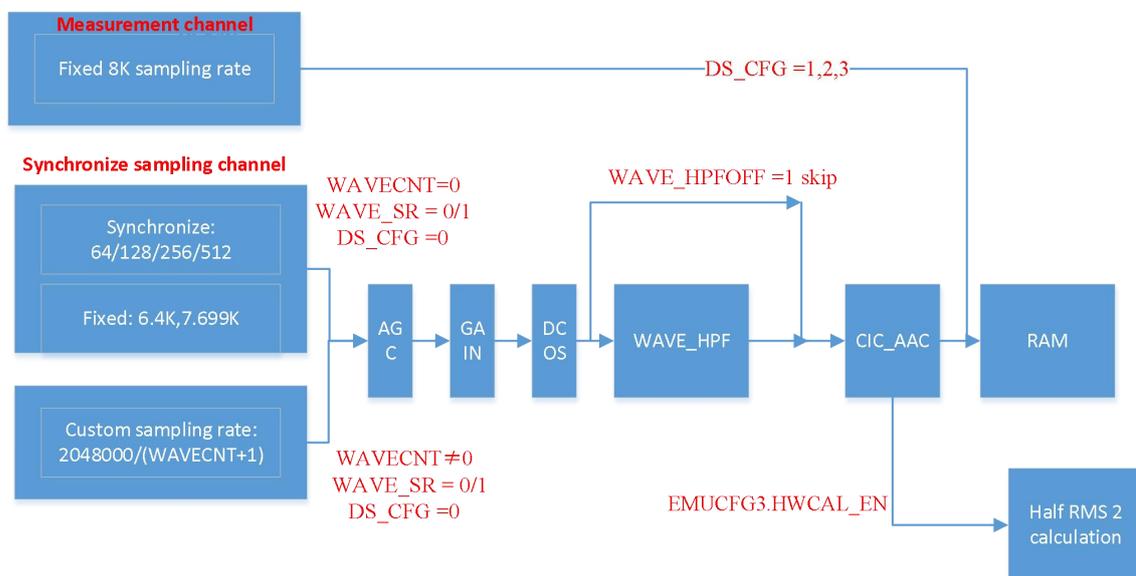
This means that before enabling the calculation of half-cycle RMS 2, it is necessary to configure the synchronous sampling channel: by DMA_WAVECON. WAVE_SR, DMA_WAVECON.DS_CFG1, WSAVECON. SWAVECFG, WSAVECON. The WFreqSEL register bits determine the number of synchronous sampling points, as described in Section 2.4.2.

- The startup point does not depend on zero-crossing and is initiated by the software configuration;

    Software configuration EMUCFG3.HWCAL_EN=1, start calculating half-cycle RMS, configure EMUCFG3.HWCAL_EN=0, stop calculating half-cycle RMS, and output half-cycle RMSs after enabling 7 channels.

- Support various standard half-cycle RMS calculations;

    Software configuration DMA_WAVECON2. HW_CLASS bits,

    =0, repeat the half-cycle wave sliding window, and the half-cycle wave updates the one-cycle RMS.
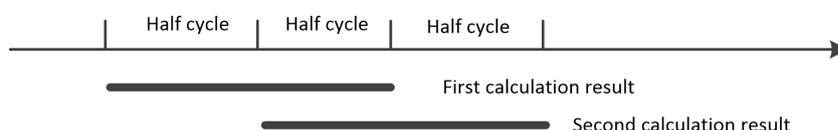
=1, no duplicate data sliding window, the HWCNT register manually configures the number of points, and the software decides whether to slide the half-cycle or one-cycle. Includes: one-cycle RMS for one-cycle updates or half-cycle RMS for half-cycle updates.
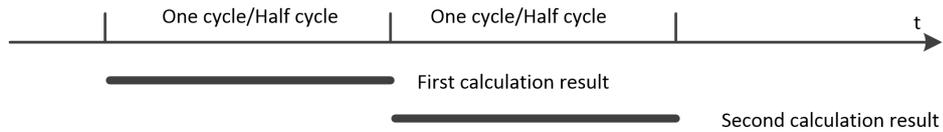
● Support 32~512 points arbitrary configuration;

By configuring the register HWCNT, any combination of the following can be achieved by means of points and sliding windows.

S1: Sum of squares of the previous half-cycle data;

S2: Sum of squares of the current half-cycle data

N: The number of half-cycle sampling points of the simultaneous sampling channel.

HW_CLASS	A half-cycle RMS calculates required the number of points HWCNT+1	Update Cycle	Calculation Formula
0	2N	Half cycle	$\sqrt{\dfrac{S1+S2}{2N}}$
1	2N	One cycle	$\sqrt{\dfrac{S1+S2}{2N}}$
1	N	Half cycle	$\sqrt{\dfrac{S2}{N}}$

2.4.9.2.1　Output

● Half-cycle RMS register 2

The output of half-cycle RMS register 2 (B0 0xC6~0xCC) is the result of setting the square root of the simultaneous sampling of the number of points (HWCNT+1), so the relationship between half-cycle RMS register 2-HW2 and RMS register RMS (B0 0x7-0xE) is: RMS=HW2 * 32/sqrt (N), where N is the set number of points (HWCNT+1). Please refer to Section 3.2.8.2 for details.

● Half-cycle RMS 2 interrupt output

The software reads EMMIF2.HW_ RMS_ If=1, it indicates that the calculation result of half RMS 2 is updated and can be read. Configure EMMIF2.HW_ RMS_ IF=1 can clear this flag. If EMMIE2.HW is enabled_ RMS_ IE=1, when EMMIF2.HW_ RMS_ When IF=1, an interrupt signal will be generated by EMMIE2.HW_ INTSEL selects INTN1 or INTN2 pin output.

2.4.11.Power Factor

The power factor register includes the total power factor PfA/PfB/PfC/PfT of the per-phase and all-phase, and the fundamental power factor FPfA/FPfB/FPfC/FPfT of the per-phase and all-phase.

Total Per-phase Power Factor: $PFx = \dfrac{P_X}{S_X}$. Where, x＝a, b, c. Sx indicates the apparent power of each per-phase, and Px indicates the active power of each per-phase, which is the signed value.

Total All-phase Power Factor: $PF_T = \dfrac{P_T}{S_T}$. Where, x = a, b, c. ST indicates the apparent power of each all-phase, and PT indicates the active power of each all-phase, which is the signed value.

The fundamental power factor is calculated by the fundamental active and fundamental apparent power parameters, and the calculation method is the same as that of the total.

For the details on the power factor register, refer to Section 3.2.4.

2.4.12. Zero-crossing Detection

Provide seven fundamental voltage and current waveform positive zero-crossing detection function, when a phase positive crossing, the corresponding zero-crossing interrupt flag EMMIF.ZXIxIF/ZXUxIF(B1 0x65[7:1]) is set, if the corresponding zero-crossing interrupt EMMIE.ZXIxIE/ZXUxIE(B1 0x64[7:1]) is enabled, a zero-crossing interrupt is generated. For the description of zero crossing interrupt enable and flag register, refer to Section 3.4.21. It should be noted that the current zero-crossing depends on the voltage zero-crossing, if there is no voltage zero-crossing, the current zero-crossing cannot be generated, but the corresponding phase voltage zero-crossing is not required. In particular, for 50Hz applications, the zero-crossing interruption is 5.5ms relative to the actual zero-crossing hysteresis. For 60Hz applications, the zero-crossing interruption is 6ms relative to the actual zero-crossing hysteresis.

Provide voltage and current zero crossing threshold register ZXOT (B1 0x05), voltage zero crossing and frequency measurement threshold register ZXOTU (B1 0x90), if the RMS of voltage and current is less than the configured zero crossing threshold, the circuit zero-crossing interrupt, phase angle, frequency measurement is not output. Current zero-crossing and phase angle calculation thresholds using ZXOT (B1 0x05) only. Voltage zero-crossing and phase angle calculation, frequency measurement threshold can choose to use ZXOT or ZXOTU, when ZXOTCFG. When ZXOTUS=1(B1 0x92), ZXOTU(B1 0x90) can be selected as the voltage zero-crossing and phase angle calculation and frequency measurement threshold. When ZXOTCFG. When ZXOTUS=0, ZXOT is selected as the voltage zero-crossing and phase angle calculation and frequency measurement threshold. Use ZXOT by default (B1 0x05).

The ZXOT register description is detailed in Section 3.4.4, the ZXOTCFG register description is detailed in Section 3.4.46, and the ZXOTU register description is detailed in Section 3.4.45.

2.4.13. Phase Angle

Provide the function of phase angle measurement among seven voltage and current. For the description and usage of seven phase angle registers YUA, YUB, YUC, YIA, YIB, YIC and YIN, refer to Chapter 3.2.7.

For the rated input (Un = 220mV, Ib = 50mV), the phase angle measurement error is less than 0.02°. The phase angle register has an update period of 32-cycle, and the angle can be changed to one-cycle by setting the control bit EMUCFG.ANGLE_FREQ.

The phase angle register is the phase angle between the fundamental and reference of each sampling channel, which are sorted by priority UA>UB>UC.

By configuring the register ZXOTCFG. ZXOTUx(x=A,B,C), users can specify in U/UB/UC whether a voltage channel participates in the phase angle operation unconditionally or through the ZXOT/ZXOTU threshold comparison result criterion. When ZXOTCFG.ZXOTUx=1, the phase voltage unconditionally participates in the phase angle operation; When ZXOTCFG. ZXOTUx=0, the phase voltage is compared with the ZXOT or ZXOTU threshold register, > ZXOT or ZXOTU, it participates in the phase angle operation, ≤ ZXOT or ZXOTU, the phase voltage does not participate in the phase angle operation. The default is 0.

For three-phase four-wire, if UA participates in phase angle operation, UA is the reference channel; If UA does not participate in phase angle operation and UB participates in phase angle operation, UB is the reference channel; If neither UA nor UB participates in phase angle operations, and UC participates in phase angle operations, UC is the reference channel. If UA, UB, and UC do not participate in the phase angle operation, the phase angle of each channel is 0.

For three-phase three-wire: via configuration register ZXOTCFG. ZXOTUBS configures whether UB participates in phase angle operations. Default ZXOTCFG. ZXOTUBS=0, UB does not participate in the phase angle operation, at this time, if UA participates in the phase angle operation, UA is the reference channel; If UA does not participate in phase angle operation and UC participates in phase angle operation, UC is the reference

channel; If neither UA nor UC participates in the phase angle operation, the phase angle of each channel is 0. If ZXOTCFG. ZXOTUBS=1, UB participates in the phase angle operation, then the three-phase three-wire and three-phase four-wire are consistent.

By configuring the register ZXOTCFG. ZXOTUS, the user can choose whether the U/UB/UC uses the ZXOT or ZXOTU register as the threshold register for zero crossing, frequency measurement, and phase angle operations, =0, select the ZXOT register; =1 to select the ZXOTU register. The default is 0.

The current phase angle calculation threshold will only use ZXOT (B1 0x05) as the zero crossing, frequency measurement, phase angle operation threshold register, when doing the phase angle operation, IA, IB, IC, IN and ZXOT threshold register comparison, > ZXOT, the current participates in the phase angle operation, ≤ ZXOT, the current does not participate in the phase angle operation, the corresponding phase angle register output is 0.

ZXOTCFG. ZXFLAG is used to store the phase angle calculation flag bits of each channel, and the flag {IN/IC/IB/IA/UC/UB/UA} of each channel indicate the channel whether participates in the phase angle calculation.

2.4.14. Voltage Line Frequency

Provide the function of the voltage line frequency measurement. For the details on the voltage line frequency register UFeq (B0 0x57), refer to <u>Section 3.2.12</u> Register. The resolution of the voltage line frequency is up to 0.0001Hz, and the measuring accuracy is up to 0.02%. Frequency measurement range: 40~70Hz.

The voltage line frequency register update period can be Freq_Cycle to one-cycle or 32-cycle by configuring the bit21 bit in register EMUCFG3 (B1 0x6D).

Frequency measurement reference:

- Three-phase four-wire: If UA>ZXOT (normalized value, ZXOTCFG can also be configured. The ZXOTUS register bit selects the ZXOTU register as the threshold, the same below), and the UA channel is used as the frequency measurement reference; If UA<ZXOT and UB>ZXOT, the UB channel is used as the frequency measurement reference</ZXOT and UB>; If UA<ZXOT and UC>ZXOT, the UC channel is used as the frequency measurement reference UC. If all three phases are less than ZXOT, the frequency register output is 0.

- Three-phase three-wire: if UA>ZXOT, the UA channel is used as the frequency measurement reference; If UA<ZXOT and UC>ZXOT, the UC channel is used as the frequency measurement reference. If both UA and UC are less than ZXOT, the frequency register output is 0.

2.4.15. Loss of Voltage Detection

Provide the loss of voltage threshold register LostVoltage (B1 0x04) and the loss of voltage state flag bit LostVoltSA, LostVoltSB and LostVoltSC (B1 0x69[0:2]) of each phase for the loss of voltage detection.

The loss of voltage threshold register LostVoltage (B1 0x04) is used to set the loss of voltage threshold of MKE304T.For the details, refer to Section 3.4.3 Register.

The loss of voltage state flag bit LostVoltSA, LostVoltSB and LostVoltSC indicate the loss of voltage judgment result of each phase. For the details on the criterion and flag bit, refer to Section 3.4.31.

2.4.16. Voltage Phase Sequence Detection

Provide the function of the voltage phase sequence error detection.

Voltage phase sequence error three-phase four-wire criterion: (1) YUBUA is outside 120°±10° (2) YUCUA is outside 240°±10°; (3)UA<ZXOT or ZXOTU (determined by ZXOTCFG. ZXOTUS configuration to use ZXOT or ZXOTU normalization value, the same below); (4) UB<ZXOT or ZXOTU; (5)UC<ZXOT or ZXOTU; If any of the above situations occur, it is judged that the three-phase four-wire voltage phase sequence is incorrect.

Three phase three wire criterion: (1) YUCBUAB is outside 300 ° ± 10 °; (2) UAB<ZXOT or ZXOTU; (3)UCB<ZXOT or ZXOTU. If any of the above situations occur, it is judged that the three-phase three-wire voltage phase sequence is incorrect.

The voltage phase sequence error flag UPhSqErr (B1 0x69[3]) indicates the detection result. The voltage phase sequence error criterion and the UPhSqErr flag are described in Section 3.4.31.

The phase sequence judgment is relatively simple, and the reverse phase sequence judgment of the meter recommends that the application use the angle to determine the zero-crossing order of each phase.

2.4.17. Voltage Sag Detection

Provide the function of the polyphase input voltage UA, UB and UC voltage sag detection.

Criterion for a phase: If the high 16-bit of the peak absolute for the voltage fundamental sample of this phase is less than SAGLVL [15:0] and the duration is SAGCYC [7:0] half cycles, it is judged as this phase voltage is sag. Of which, SAGLVL [15:0] is the low 16-bit of the voltage sag threshold register SAGCFG (B1 0x58), and SAGCYC [7:0] is the high 8-bit of SAGCFG (B1 0x58).For the details on the SAGCFG register, refer to Section 3.4.14.

The voltage sag of a phase will cause the bit of the SAGUx (x=A, B, C) register for this phase in the PHASES register (B1 0x69) is set to 1, and the bit of the SAGIF register in the EMMIF register (B1 0x64) is set to 1. If SAGIE=1 in the EMMIE (B1 0x65) register, setting SAGIF to 1 will interrupt INT. It will clear this interrupt when clear SAGIF. At the same time, it will clear the SAGUx flag in the PHASES register. This mode is only available for MODESEL=0 three-phase four-wire mode.

If EMUCFG.SAGINT_CFG(B1 0x61[15])=1 and EMUIE.SAGIE (B1 0x65)=1, when MODESEL=0 is configured as a three-phase four-wire, a polyphase PHASES.SAGUx (B1 0x69) is set to 1 to cause EMUIF.SAGIF (B1 0x64) to be set to 1, and a SAG interrupt will be generated. When MODESEL=1 is configured as a three-phase three-wire, SAGUA and SAGUC are both set to 1 to cause EMUIF. SAGIF is set to 1 and generates a SAG interrupt at the same time.

There are SAG_UxPEAK register banks (Bank0 C3H~C5H) to record the minimum of the absolute of all voltage half-cycle peaks in each phase during the SAG event. For the details on SAG_UxPEAK registers, refer to Section 3.2.14.

For the details on the PHASES register, refer to Section 3.4.31. For the details on the bit of the SAGIE register and the bit of the SAGIF register, refer to Section 3.4.27.1, Section 3.4.27.2 and Chapter 2.7 Interrupt.

2.4.18. Voltage Sag Detection 2

Provide a voltage sag threshold register LVDCFG (B1 0xE7) for voltage sag detection 2.

The voltage sag detection 2 module does not depend on zero crossing, the data source takes the 8KHz waveform after high-pass filter, and the half-cycle directly fixes the number of points, 50Hz corresponds to 80 points, and 60Hz corresponds to 67 points. When comparing durations, record the number of half-cycle numbers every 80 or 67 points, and the cumulative half-cycle numbers are compared with LVDCFG.CNTTH. 50Hz/60Hz selection by EMUCFG. FREQ_SEL configuration.

The voltage sag detection 2 module event triggers:

Three-phase four-wire: A/B/C three phases are all judged to be voltage sag states, LVD event triggers, EMMIF2. LVD_IF flag flipped, if enabled EMMIE2.LVD_IE, the EMMIE2.LVD_INTSEL configuration outputs an interrupt signal from the INTN1/INTN2 pins;

Three-phase three-wire: A/C two-phase all judged to be voltage sag state, LVD event triggered, EMMIF2. LVD_IF flag flipped, if enabled EMMIE2.LVD_IE, the EMMIE2.LVD_INTSEL configuration outputs an interrupt signal from the INTN1/INTN2 pins. The selection of three-phase four-wire/three-phase three-wire is configured by the MODSEL register。

When the absolute of the voltage half-cycle peak is less than the LVD peak threshold set by LVDCFG.PEAKTH, it is recorded as the start of event judgment, as long as the absolute of the peak of the voltage waveform is not greater than the set threshold + hysteresis threshold (PEAKTH+hysteresis), and the hold time is greater than LVDCFG.CNTTH sets the half-cycle wavenumber, it is judged that the phase is in a voltage sag state. If the three-phase four-wire UA/UB/UC is in a state of loss of voltage, it is judged that an LVD event occurs; If the three-phase three-wire UA/UC are in a state of loss of voltage, it is judged that an LVD event occurs. The loss of voltage state determination is shown in the figure:
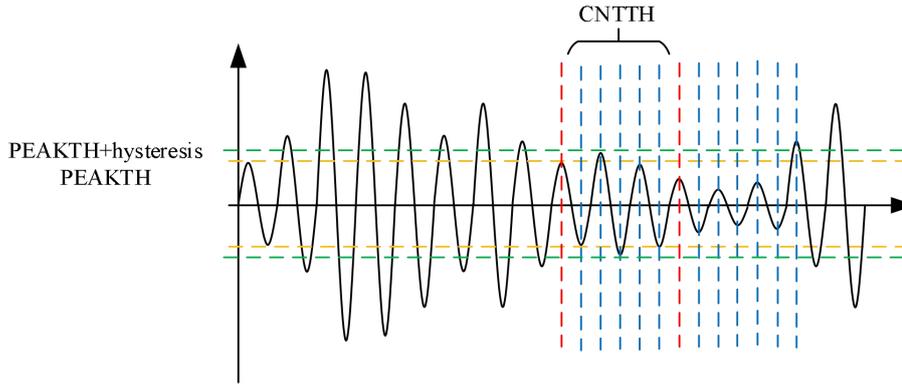
2.4.19. Overvoltage detection and voltage half-cycle peak

Provide two sets of overvoltage judgment functions for polyphase input voltage.

Overvoltage criterion 1: When the absolute of a phase voltage sampling is 16 bits higher than the overvoltage threshold register OVLVL(B1 0x59), the phase voltage is overvoltage. For the details on OVLVL register, refer to Section 3.4.16.1.

A phase voltage overvoltage will cause both the phase OVUx(x=A,B,C) register bit in the PHASES register (B1 0x69) and the OVIIF register in the EMMIF register set to 1. If OVIIE = 1 in the EMMIE register, setting OVIIF to 1 causes an interrupt. Clearing the OVIIF will clear the interrupt and clear the OVUx flag in the PHASES register.

The PHASES register is described in Section 3.4.31. OVIIE register bits and OVIIF register bits are described in Section 3.4.21.

OverVoltage criterion 2: The upper 16 bits of the absolute of the phase voltage waveform half-cycle peak UxPEAK_HW [15:0] (B0 0xA6~0xA8) is greater than the overvoltage amplitude threshold register OV2_LVL [15:0] (Bank1 0x 9C), and the overvoltage duration is greater than or equal to (the overvoltage time threshold register OV2 _CNTTH [15:0] (Bank1 0x9D))*half-cycle, then determine the overvoltage of this phase voltage.

A phase voltage overvoltage will cause the EMMIF2.OVx_IF(x=A,B,C) (Bank1 0x6C[5:3]) flag to be asserted, and if EMMIE2.OVx _IE (Bank1 0x6B[5:3]) = 1, an overvoltage interrupt will occur.

In order to ensure the accuracy of the half-cycle time count, the user needs to configure EMUCFG. FREQ_SEL (Bank1 0x61[11]) for 50Hz/60Hz application configurations.

Conditions for turning on the polyphase voltage overvoltage detection function: OV2_LVL [15:0] ≠0 and OV2_CNTTH [15:0] ≠0; Conditions for turning off the polyphase voltage overvoltage detection function: OV2_LVL [15:0] =0 or OV2_CNTTH[15:0] =0.

OV2_LVL, OV2_CNTTH, and UxPEAK_HW register descriptions are described in Sections 3.4.16.2, 3.4.16.3, and 3.2.14. EMMIE2. OVx_IE, EMMIF2. OVx_IF registers are described in Section 3.4.21.3.

Related registers: channel gain register GSUx, EMUCFG. FREQ_SEL (50Hz/60Hz selection).

2.4.20. Overcurrent Detection

Provide an overcurrent judgment function for the polyphase current input.

OverCurrent criterion 1: When the absolute of the current sampling of a phase is 16 bits higher than the overcurrent threshold register OILVL(0x60), the current of the phase is determined. The OILVL register is described in Section 3.4.16.4.

A phase voltage overcurrent will result in both the phase OVIx(x=A,B,C) register bits in the PHASES register (B1 0x69) and the OVIIF register bits in the EMMIF register set to 1. If OVIIE = 1 in the EMMIE register, setting OVIIF to 1 causes an interrupt. Clearing the OVIIF will clear the interrupt and clear the OVIx flag in the PHASES register.

The PHASES register is described in Section 3.4.25. OVIIE register bits and OVIIF register bits are described in Sections 3.4.21.3 and Chapter 2.7 Interrupts.

2.4.21.Short-circuit Instantaneous Current Overcurrent Detection

Provide the function of short-circuit instantaneous current overcurrent detection, and the overcurrent amplitude and time threshold can be configured, and the short-circuit instantaneous current overcurrent interrupt is occurred when the threshold is exceeded.
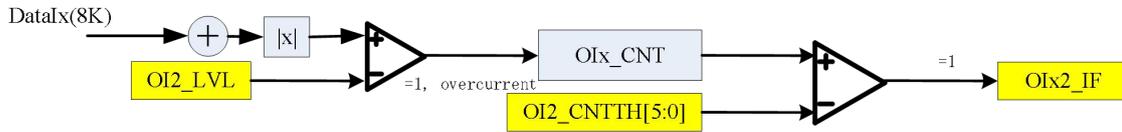
As shown in the figure, DATAIx(x=A,B,C) is an 8K instantaneous voltage waveform from a phase current ADC where the upper 16 bits of the absolute of the instantaneous value of the phase current are greater than the overcurrent amplitude threshold register OI2_LVL [15:0] (Bank1 0x98), and the internal OIx2_CNT is started and increased by 1 at 8Khz. When the cumulative count OIx2_CNT count value is greater than or equal to the pReset of the overvoltage time threshold register OI2 _CNTTH[5:0] (Bank1 0x99), the phase current is determined to be short-circuited and overcurrent, and the EMMIF2.OIx2_IF (x=A,B,C) (Bank1 0x6C[2:0]) flag of the corresponding phase is set, if the corresponding phase EMMIE2.OIx2_IE (Bank1 0x6B[5:3]) overcurrent interrupt enabled, The phase short-circuit is shorted and the current is interrupted instantaneously.

Conditions for turning on the polyphase voltage overcurrent detection function: OI2_LVL [15:0]≠0 and OI2_CNTTH[5:0] ≠0; Conditions for turning off the polyphase voltage overcurrent detection function: OI2_LVL[15:0]=0 or OI2_CNTTH[5:0]=0.

Determine the conditions for the current overcurrent of a certain phase:

1. The absolute of the instantaneous sampling of the phase 8K current is 16 bits higher than the current threshold register OI2_LVL [15:0];

2. The cumulative time greater than OI2_LVL [15:0] exceeds OIx2_CNTTH [5:0]*(1/8) ms;

OIx_CNT counter clearance condition:

1.OIx_IF software writes 1 to clear the interrupt and clear the counter;

2.If the overcurrent current threshold is exceeded, the count is started, and the counter is cleared below the overcurrent current threshold OIx_CNT;

3.Turn off the polyphase short-term transient current overcurrent detection function;

OI2_LVL. The description of OI2_CNTTH registers is detailed in Sections 3.4.16.5 and 3.4.16.6. EMMIE2. OIx2_IE, EMMIF2. OIx2_IF registers are described in Section 3.4.21.

Related register: Channel gain register GSIx.

2.4.22.Flickering

Provide polyphase voltage transient flicker calculation, the register FLK_Ux save 5 instantaneous voltage samplings for each channel within 10ms, each time 500Hz update, the user can read according to the 10ms FIFO update frequency for flicker software calculation. FLK_RSLTx save 1 flicker calculation result for each channel, each time 500Hz update, the software needs to read it regularly.

Whether it is the instantaneous sampling of the voltage or the value of the flicker calculation result, each time the user reads away 4 bytes of 1 flicker value data, the FIFO reads the pointer by adding 1 until the pointer points to the last 4 bytes of the FIFO address, and then reads away 4 bytes, and the pointer returns to the FIFO start address. The instantaneous flicker value registers are described in Section 3.2.15.

The FIFO buffer is 20 bytes total, the FIFO write pointer returns to the FIFO start address, and the flicker buffer total flag EMMIF2.FLK_IF set. If interrupt is enabled, the buffer is total of interrupt EMMIE2.FLK_IE output, the user can read the instantaneous flicker value of each channel in turn according to the received interrupt signal, in order to prevent the FIFO write pointer from catching up with the read pointer during the user's read operation, resulting in the output error flag of the flicker module EMMIF2.FLK_ERR_IF set up (interrupt enable can output the wrong interrupt signal EMMIE2.FLK_ERR_IE), the result of the flicker calculation can be read 5 times in order, such as: UA-UB-UC-UA-UB-UC-UA...... The SPI read sequence is shown in the dotted line below, and the flicker interrupt register details are described in Section 3.4.21.3.
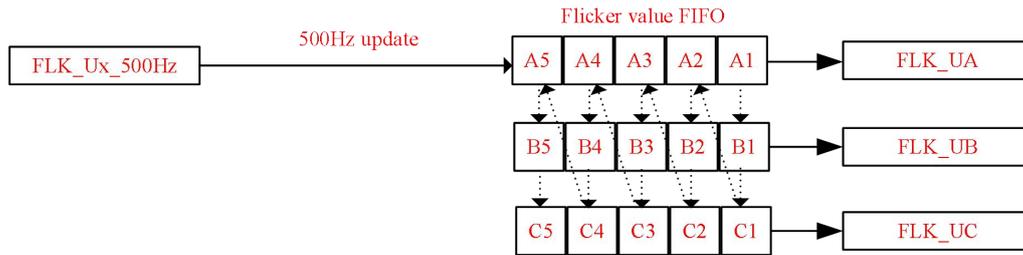
Whether it is the voltage instantaneous sampling or the flicker calculation result stored in the FLK_RSLTx register, each time the user can only read away 4 bytes of 1 flicker value data, there is no FIFO buffer mechanism, and the user needs to time 500Hz frequency to read, otherwise it will be overwritten.
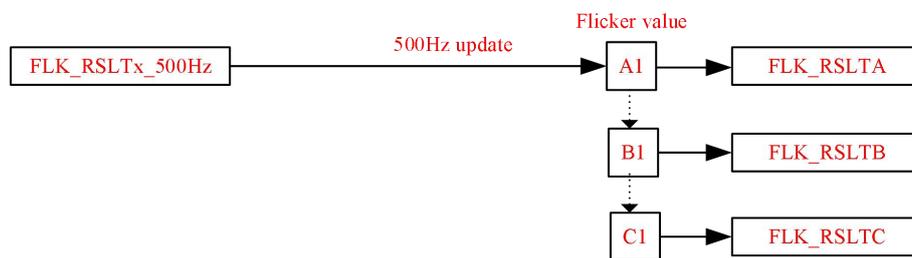
If the flicker error flag is set to 1, the flicker module is turned off and you need to perform flicker calculation again, configure EMUCFG3.FLKCAL_EN enable flicker module to calculate, and the flicker module computing unit is reset. The flicker calculation enablement is detailed in Section 3.4.18.3. Flicker clock gating configuration SYSCFG.FLK_CK_EN, clock start, module enable, clock off, module zero, refer to Section 3.4.34 for details.

2.5. Low Power Mode

Provide the no-voltage mode 1 (NVM1) to measure the low power current RMS and the no-voltage mode 2 (NVM2) to pre-judge the low power no-voltage current, and judges the no-voltage accurately by current RMS. Furthermore, it will Supplies sleep mode (SLM), which is used in the sleep status when the electrical energy meter is powered by the backup battery after the power grid is powered down.

Users can combine with NVM1, NVM2 and SLM, to complete each phase currents judgment and the current RMS measurement of the no-voltage. For the details, refer to the application note MKE304T No-voltage Measurement Function.

2.5.1. No-voltage Mode 1

The no-voltage mode 1 (NVM1) is used to measure the low power current RMS and judge the no-voltage accurately by current RMS.

Under NVM1, the chip contains a polyphase RMS current measurement unit, and the results are output to the 3-phase RMS current register under NVM1 25Hz update register IA_NVM1 (B0 0x11), IB_NVM1 (B0 0x12), IC_NVM1 (B0 0x13), and single update register RMS_LA1 (B0 0xBD), RMS_LB1 (B0 0xBE), RMS_LC1 (B0 0xBF), The registers are described in Section 3.2.2.

The error over the 400:1 range of the current RMS in the NVM1 mode is less than 0.5%.

In other operating modes, the chip writes the GONVM1 command to the operating mode switching register WMSW (B1 0x81) under write-enable conditions, and the chip automatically switches to NVM1 and starts the RMS current calculation.

When the HPFOFF register bit in the NVM1CFG register (B1 0x70) = 0, that is, when the high-pass filter is turned on, the settling time of the no-voltage RMS measurement is 1.6s; When HPFOFF=1, that is, when the high-pass filter is off, the settling time of the no-voltage RMS measurement is 80ms, at this time, the user can use the

dc OFFSET automatic calibration function to calculate the DC OFFSET calibration register of the three currents to replace the high-pass filter to eliminate the offset error AUTODC_EN. EMM_DC_DIS=1(B1 0x91 [7]), the DCOS register only affects NVM1 RMS current calculation, and the automatic calibration is initiated by IA_DC_EN, IB_DC_EN, and IC_DC_EN, and the obtained value is filled into the LS_DCOS register. Refer to Section 3.4.6.15 for instructions.

After the NVM1 RMS current register is stabilized, the user-readable RMS current register perfoRMS no-voltage judgment.

The NVM1IE bit in the NVM1CFG register (B1 0x70) configures interrupt enable shutdown under NVM1. NVM1IF register (B1 0x71) NVM1Done is asserted after switching, and if NVM1IE=1, an interrupt is generated.

The NVM1CMPIE bit enables no-voltage in the NVM1CFG register (B1 0x70) to complete the comparison interrupt. The no-voltage is calculated and at least one I channel exceeds the set threshold, the NVM1IF register (B1 0x71) NVM1CMPDone flag is asserted, and the corresponding channel NVM1CMPxDone flag is asserted. If NVM1CMPIE=1, an interrupt is generated. The calculation time is configured by LS_THOx (B1 0xCE~0xD0 [23:22]) polyphase four-step, when the polyphase RMS current register Ix_NVM1 [21:0]≥LS_THOx [21:0] or Ix_NVM1[22]=1, the threshold is exceeded, and the no-voltage measurement threshold setting register is described in Section 3.4.3.16.

The NVM1UDIE bit in the NVM1CFG register (B1 0x70) enables no-voltage calculation of RMS update at a fixed frequency (25Hz). After the no-voltage calculation of RMS is updated, the NVM1UDIF flag in the NVM1IF register (B1 0x71) is set, and if NVM1UDIE=1, an interrupt is generated.

The NVM1CFG registers are described in Section 3.4.33.1. The NVM1IF register is described in Section 3.4.33.2.

2.5.2. No-voltage Mode 2

The no-voltage mode 2 (NVM2) is used to pre-judge the low power no-voltage current.

Include the polyphase current comparison unit in the NVM2 mode, to compare the polyphase input current and the comparison unit threshold. Two levels of the comparison unit threshold are optional and can be configured by the bit of the NVM2TH [1:0] register in the NVM2CFG register (0x72).

The chip can configure the current comparison cycle in the NVM2 mode by the bit of the NVM2TNUM[4:0] register in the NVM2CFG register (0x72).

The chip can configure the interrupt enable closure in the NVM2 mode by the bit of the NVM2IE register in the NVM2CFG register (0x72).For the details on the NVM2CFG register, refer to Section 3.4.34.1.

Three registers NVM2CMP A/B/C (0x73-75) are used to output and process three comparators in the NVM2 mode. It shall be initialized as 0x0000 during the normal use. For the details on the register, refer to Section 3.4.34.2.

After configure above register in other operating modes (such as SLM, EMM and NVM1), write the GONVM2 command into the operating mode switching register (0x81) in the Write Enable condition. The MKE304T is switched to NVM2 automatically and enables the comparison of the polyphase input current for one time by the NVM2CFG register configuration. The comparison result is stored in the NVM2IF register (0x76) after NVM2TNUM [4:0] + 1 cycles. If NVM2IE=1, the bit of the NVM2Done (NVM2IF.0) register is set upon completion of the comparison of the polyphase input current and causes the interrupt. For the details on the NVM2IF register, refer to Section 3.4.34.3 and Chapter 2.7.

2.5.3. Sleep Mode

The SPI and AVCC power supply monitoring operate only in the sleep mode, and users can read and write NVM1, NVM2 and System Configuration and Status Register by SPI.

When the external pin PM is configured to 1 and power-up reset, the system is in the SLM mode.

After the GOEMM, GONVM1 and GONVM2 command are written into the Operating Mode Switching Register (0x81) in the SLM mode in the Write Enable condition, The MKE304T is switched to EMM, NVM1 and NVM2 automatically.

After the GOSLM command are written into the Operating Mode Switching Register (0x81) in other operating modes in the Write Enable condition, switch to SLM automatically.

2.6. ADCIN Mode

ADCIN mode differs from EMM mode only in whether or not the ADC is external. In ADCIN mode, there are two polyphase shunt meter applications. Application 1: Four-channel current channel ADC external, three-channel voltage channel ADC internal; Application 2: All seven ADCs are external. There are two package types (LQFP44 and LQFP32) on the chip, LQFP32 lacks the configuration to enter the ADCIN mode pin, which requires software configuration to enter, and the two package types configure the ADCIN mode of the two schemes as shown in the following table:

Packaging type	Application 1	Application 2
LQFP44 Software + Pins	Pins: 1.ADIN_MOD=1; 2.PM=0 Software: 3.Bank1 0x80H write 0xE5; 4.Bank1 0xA1H write 0xEA; 5.Bank1 0xA0H write 0x1040; Software reliability: 7.Read Bank1 0xA0H as 0x1040	Pins: 1.ADIN_MOD=1; 2.PM=0; Software: 3.Bank1 0x80H write 0xE5; 4.Bank1 0xA1H write 0xEA; 5.Bank1 0xA0H write 0x0040; Software reliability: 6.Read Bank1 0xA0H as 0x0040.

Before configuring ADCIN mode, you need to configure the write-protect register ADCIN_WREN (Bank1 A1H), enable the ADCIN mode configuration register ADCIN_CFG (Bank1 A0H), and ADCIN_CFG. ADCIN_UADC register bits selectable U-channel 1-bit source (i.e., U-channel ADC internal/external); ADCIN_CFG. ADCIN_SOFT_EN register bits, only for the LQFP32 package, and ADCIN mode switching can only be completed by software in EMM mode; ADCIN_CFG. ADCxx_PUT register bits can be individually configured for each channel ADC internal/external. The ADCIN mode registers are detailed in Sections 3.4.36.2 and 3.4.36.3.

2.7. Interrupt

The chip interrupt is summarized as shown in the table below.

Table 2-6-1: Interrupt in EMM Mode

No:	Interrupt	Description	Interrupt Enable	Interrupt Flag
39	LVD events generate interrupt	The three-phase four-wire U/UB/UC are all in a lost-voltage state, and the LVD event flag is flipped, and if EMMIE2.bit25 is enabled, it will cause the INT pin to flip from high to low.	LVD_IE	LVD_IF
38	Simultaneous sampling half-cycle RMS 2 update interrupt	The half-cycle RMS 2 register of the synchronous sampling channel is updated, and the flag position 1.If the EMUIE2 bit24 enable is interrupted, it will cause the INTN pin to flip from high to low。	HW_RMS_IE	HW_RMS_IF
37	Automatic	One of the 7 channels of automatic temperature	AUTOECT_G	AUTOECT_G

	error temperature compensation gain factor update interrupt	compensation has a gain factor update event in the high or low temperature segment, and this flag is asserted, and if enabled is interrupted, it will cause the INTN pin to flip from high to low. Write 1 to AUTOECT_GAINUDIF and clear interrupt.	AINUDIF	AINUDIE
36	Automatic error temperature compensation out-of-bounds interrupt	An error out-of-bounds event occurs on one of the 7 channels of auto-temperature compensation, and this flag assertion, if enabled interrupts, causes the INTN pin to flip from high to low. Write 1 to AUTOECT_ERREL_IF and clear interrupt.	AUTOECT_E RREL_IF	AUTOECT_E RREL
35	HSDC outputs the busy flag	HSDC waveform output busy flag (HSDC_BUSY = 1 is recommended not to turn off HSDC_EN enable)	---	HSDC_BUSY
34	LVD events generate interrupt	The three-phase four-wire U/UB/UC are all out of voltage, and the LVD event flag is flipped, and if EMMIE2.bit25 is enabled, it will cause the INT pin to flip from high to low.	LVD_IE	LVD_IF
33	Automatic error temperature compensation gain factor update interrupt	One of the 7 channels of automatic temperature compensation has a gain factor update event in the high or low temperature segment, and this flag is asserted, and if enabled is interrupted, it will cause the INTN pin to flip from high to low. Write 1 to AUTOECT_GAINUDIF and clear interrupt.	AUTOECT_G AINUDIF	AUTOECT_G AINUDIE
32	Automatic error temperature compensation out-of-bounds interrupt	An error out-of-bounds event occurs on one of the 7 channels of auto-temperature compensation, and this flag assertion, if enabled interrupts, causes the INTN pin to flip from high to low. Write 1 to AUTOECT_ERREL_IF and clear interrupt.	AUTOECT_E RREL_IF	AUTOECT_E RREL
31	IN channel half-cycle RMS update flag	IN channel half-cycle RMS update flag, configuration EMU_CFG. FREQ_SEL=0, that is, the update time is 10ms when 50Hz is applied, and the configuration is EMU_CFG. FREQ_SEL=1, that is, the update time is 8.3333ms when 60Hz is applied, write 1 and clear.	---	HW_ZXIN
30	UC channel half-cycle RMS update flag	UC channel half-cycle RMS update flag, configuration EMU_CFG. FREQ_SEL=0, that is, the update time is 10ms when 50Hz is applied, and the configuration is EMU_CFG. FREQ_SEL=1, that is, the update time is 8.3333ms when 60Hz is applied, write 1 and clear.	---	HW_ZXUC
29	UB channel half-cycle RMS update	UB channel half-cycle RMS update flag, configuration EMU_CFG. FREQ_SEL=0, that is, the update time is 10ms when 50Hz is applied,	---	HW_ZXUB

	flag	and the configuration is EMU_CFG. FREQ_SEL=1, that is, the update time is 8.3333ms when 60Hz is applied, write 1 and clear.		
28	UA channel half-cycle RMS update flag	UA channel half-cycle RMS update flag, configuration EMU_CFG. FREQ_SEL=0, that is, the update time is 10ms when 50Hz is applied, and the configuration is EMU_CFG. FREQ_SEL=1, that is, the update time is 8.3333ms when 60Hz is applied, write 1 and clear.	---	HW_ZXUA
27	The flicker module outputs an error interrupt	When the FLK_FIFO write pointer catches up with the SPI read pointer, the FLK_ERR_IF flag flips, and if FLK_ERR_IE = 1, the INT pin is flipped from high to low. Write 1 to FLK_ERR_IF and clear interrupt.	FLK_ERR_IE	FLK_ERR_IF
26	Flicker FIFO buffer total interrupt	The flicker FIFO stores 5 flicker results of 10ms refresh, and for every 5 results, the FLK_IF flag is flipped, and if FLK_IE = 1, it will cause the INTN pin to flip from high to low. Write 1 to FLK_IF and clear interrupt.	FLK_IE	FLK_IF
25	Waveform buffer total interrupt	When the buffer data length of synchronous sampling waveform buffer mode 0 occupies the entire open buffer space, the WAVE_FIF flag flips, and if WAVE_FIE=1, it will cause the INTN pin to flip from high to low. Write 1 to WAVE_FIF and clear the interrupt at the same time.	WAVE_FIE	WAVE_FIF
24	Waveform buffer half-total interrupt	When the buffer data length of synchronous sampling waveform buffer mode 1 and mode 2 occupies half of the open buffer space, the WAVE_HFIF flag is flipped, and if WAVE_HFIE=1, it will cause the INTN pin to flip from high to low. WAVE_HFIF Write 1 and clear interrupts at the same time.	WAVE_HFIE	WAVE_HFIF
23	Phase C voltage sag interrupt	When the voltage sag occurs in the C phase, the UC_SAGIF is set to 1, and if UC_SAGIE=1, it will cause the INTN pin to flip from high to low. UC_SAGIF write 1 to clears the interrupt at the same time, but does not clear the SAGUC status flag bit in the PHASES status register.	UC_SAGIE	UC_SBGIF
22	Phase B voltage sag interrupt	When the voltage sag occurs in phase B, UB_SAGIF set to 1, and if UB_SAGIE=1, it will cause the INTN pin to flip from high to low. UB_SAGIF write 1 to clears the interrupt at the same time, but does not clear the SAGUB status flag bit in the PHASES status register.	UB_SAGIE	UB_SBGIF

21	Phase A voltage sag interrupt	When a voltage sag occurs in phase A, UA_SAGIF set to 1, and if UA_SAGIE=1, it will cause the INTN pin to flip from high to low. Write 1 to UA_SAGIF and clear the interrupt at the same time, but does not clear the SAGUA status flag bit in the PHASES status register.	UA_SAGIE	UA_SAGIF
20	Overcurrent interruption for a short circuit of the C-phase current	When an overcurrent occurs in the C phase, OVC_IF set to 1, and if OVC_IE=1, it will cause the INT pin to flip from high to low. Write 1 to OVC_IF the interrupt at the same time. Note: This interrupt can be set and generated independently from interrupt 15.	OVC_IE	OVC_IF
19	Overcurrent interruption for a short circuit of the B-phase current	When an overcurrent occurs in phase B, OVB_IF set to 1, and if OVB_IE=1, it will cause the INT pin to flip from high to low. Write 1 to OVB_IF and clear interrupt at the same time. Note: This interrupt can be set and generated independently from interrupt 15.	OVB_IE	OVB_IF
18	Overcurrent interruption for a short circuit of the A-phase current	When an overcurrent occurs in phase A, OVA_IF set to 1, and if OVA_IE=1, it will cause the INT pin to flip from high to low. Write 1 to OVA_IF and clear the interrupt at the same time. Note: This interrupt can be set and generated independently from interrupt 15.	OVA_IE	OVA_IF
17	Overcurrent interruption for a short circuit of the C-phase current	When an overcurrent occurs in the C phase, OIC2_IF 1, and if OIC2_IE=1, it will cause the INTN pin to flip from high to low. Write 1 to OIC2_IF and clears interrupts at the same time. Note: This interrupt can be set and generated independently from interrupt 15.	OIC2_IE	OIC2_IF
16	Overcurrent interruption for a short circuit of the B-phase current	When an overcurrent occurs in phase B, OIB2_IF set to 1, and if OIB2_IE=1, it will cause the INTN pin to flip from high to low. Write 1 to OIB2_IF the interrupt at the same time. Note: This interrupt can be set and generated independently from interrupt 15.	OIB2_IE	OIB2_IF
15	Overcurrent interruption for	When an overcurrent occurs in phase A, OIA2_IF set to 1, and if OIA2_IE=1, it will cause the	OIA2_IE	OIA2_IF

	a short circuit of the A-phase current	INTN pin to flip from high to low. Write 1 to OIA2_IF and clear interrupts at the same time. Note: This interrupt can be set and generated independently from interrupt 15.		
16	Overvoltage and Overcurrent Interrupt	When any phase of the polyphase voltage is overvoltage or any phase of the polyphase current is overcurrent, OVIIF is set to 1.If OVIE = 1, it will cause the INTN pin is toggled from high to low. OVIIF writes 1 and clears 0, and clears the interrupt and the OVUA, OVUB, OVUC, OIIA, OIIB and OIIC status flag bits in the PHASES status register.	OVIIE	OVIIF
17	Voltage Sag Interrupt	When any phase of the polyphase voltage sags, SAGIF is set to 1.If SAGIE = 1, it will cause the INTN pin is toggled from high to low. Write 1 to SAGIF and clear the interrupt and the SAGUA, SAGUB and SAGUC status flag bits in the PHASES status register.	SAGIE	SAGIF
18	Status Change Interrupt of Current Segment 3	When any phase of current RMS for three phases A/B/C changes compared to the segment status set by IRegion3H/IRegion3L, IRegion3IF is set to 1. Query the Regions register further, to confirm which segment status of the current RMS changes. If IRegion3IE = 1, it will cause the INTN pin is toggled from high to low.IRegion3IF writes 1 and clears 0, and clears the interrupt at the same time.	IRegion3IE	IRegion3IF
19	CF4 Pulse Output Interrupt	CF4 outputs the pulse, and the output changes into the high level from the low level. CF4IF is set to 1.If CF4IE = 1, it will cause the INTN pin is toggled from high level to low level. Write 1 to CF4IF and clear interrupt at the same time.	CF4IE	CF4IF
20	CF3 Pulse Output Interrupt	CF3 outputs the pulse, and the output changes into the high level from the low level. CF3IF is set to 1.If CF3IE = 1, it will cause the INTN pin is toggled from high level to low level. Writes 1 to CF3IF and clear interrupt at the same time..	CF3IE	CF3IF
21	CF2 Pulse Output Interrupt	CF2 outputs the pulse, and the output changes into the high level from the low level. CF2IF is set to 1.If C2IE = 1, it will cause the INTN pin is	CF2IE	CF2IF

		toggled from high level to low level. Writes 1 to CF2IF and clear interrupt at the same time.		
22	CF1 Pulse Output Interrupt	CF1 outputs the pulse, and the output changes into the high level from the low level. CF1IF is set to 1.If C1IE = 1, it will cause the INTN pin is toggled from high level to low level. Writes 1 to CF1IF and clear interrupt at the same time.	CF1IE	CF1IF
23	IN Positive Zero-crossing Interrupt	When IN > ZXOT and IN is positive zero-crossing, ZXINIF is set to 1.If ZXINIE = 1, it will cause the INTN pin is toggled from high level to low level. Write 1 to ZXINI and clear interrupt at the same time.	ZXINIE	ZXINIF
24	IC Positive Zero-crossing Interrupt	When IC > ZXOT and IC is positive zero-crossing, ZXICIF is set to 1.If ZXICIE = 1, it will cause the INTN pin is toggled from high level to low level. Write 1 to ZXICIF and clear interrupt at the same time.	ZXICIE	ZXICIF
25	IB Positive Zero-crossing Interrupt	When IB > ZXOT and IB is positive zero-crossing, ZXIBIF is set to 1.If ZXIBIE = 1, it will cause the INTN pin is toggled from high level to low level. Write 1 to ZXIBIF and clear interrupt at the same time.	ZXIBIE	ZXIBIF
26	IA Positive Zero-crossing Interrupt	When IA > ZXOT and IA is positive zero-crossing, ZXIAIF is set to 1.If ZXIAIE = 1, it will cause the INTN pin is toggled from high level to low level. Writes 1 to ZXIAIF and clears interrupt at the same time.	ZXIAIE	ZXIAIF
27	UC Positive Zero-crossing Interrupt	When UC > ZXOT and UC is positive zero-crossing, ZXUCIF is set to 1.If ZXUCIE = 1, it will cause the INTN pin is toggled from high level to low level. Write 1 to ZXUCIF and clears interrupt at the same time..	ZXUCIE	ZXUCIF
28	UB Positive Zero-crossing Interrupt	When UB > ZXOT and UB is positive zero-crossing, ZXUBIF is set to 1.If ZXUBIE = 1, it will cause the INTN pin is toggled from high level to low level. Writes 1 to ZXUBIF and clear interrupt at the same time..	ZXUBIE	ZXUBIF
29	UA Positive Zero-crossing Interrupt	When UA > ZXOT and UA is positive zero-crossing, ZXUAIF is set to 1.If ZXUAIE = 1, it will cause the INTN pin is toggled from high level to low level. Writes 1 to ZXUAIF and clears interrupt at the same time..	ZXUAIE	ZXUAIF
30	Waveform Sampling	It synchronizes the 8Khz rate refresh with the waveform sampling register. WAVUDIF writes 1	WAVUDIE	WAVUDIF

	Interrupt	and clears 0.If WAVUDIE = 1, clear and clears interrupt at the same time.		

Table 2-6-2 Interrupt in NVM1 Mode of MKE304T

No:	Interrupt	Description	Interrupt Enable	Interrupt Flag
3	NVM1 threshold compares overflow interrupts	No-voltage is calculated and at least one I channel exceeds the set threshold to produce an interrupt. This interrupt is only valid in NVM1 mode and not in other modes.	NVM1CMPIE	NVM1CMPDone,NVM 1CMPADone,NVM1C OMPBDone,NVM1CO MPCDone
2	NVM1 fixed frequency update interrupts	No-voltage of calculation RMS fixed frequency update (25Hz)interrupt enable;	NVM1UDIE	NVM1UDIF
1	NVM1 Mode Switching	Refer to the chapter NVM1IE and NVM1IF.	NVM1IE	NVM1Done

Table 2-6-3 Interrupt in NVM2 Mode of MKE304T

No:	Interrupt	Description	Interrupt Enable	Interrupt Flag
1	Completion of NVM 2 Mode Switching and Current Comparison	Refer to the chapter NVM2 IE and NVM2IF.	NVM 2IE	NVM 2Done

Note:

1.The MKE304T Interrupt Related to Operating Mode: The interrupt in the EMM mode doesn't play any role in the low power mode. The NVM1 interrupt plays its role in the NVM1 mode only, and the NVM2 interrupt plays its role in the NVM2 mode only, but doesn't play any role in any other modes.

2.IF is both the status register and the interrupt flag register. IF is not controlled by the IE interrupt Enable.

3.Register

3.1.Parameter Register List

Table 3-1 Parameter Register (Bank0, refer to Section 5.1 for address mappings) List

Address	Name	R/W	Byte Length	EMM Power-up Reset	Description
Total Measurement Parameter Register					
00H	UAWAV	R	3	--	Voltage sampling data of phase A
01H	UBWAV	R	3	--	Voltage sampling data of phase B
02H	UCWAV	R	3	--	Voltage sampling data of phase C
03H	IAWAV	R	3	--	Current sampling data of phase A
04H	IBWAV	R	3	--	Current sampling data of phase B
05H	ICWAV	R	3	--	Current sampling data of phase C
06H	INWAV	R	3	--	Null current sampling data
07H	UA	R	4	--	Voltage RMS of phase A
08H	UB	R	4	--	Voltage RMS of phase B
09H	UC	R	4	--	Voltage RMS of phase C
0AH	USUM	R	4	--	Voltage vector sum RMS
0BH	IA	R	4	--	Current RMS of phase A
0CH	IB	R	4	--	Current RMS of phase B
0DH	IC	R	4	--	Current RMS of phase C
0EH	IN	R	4	--	Null current RMS
0FH	Reserved			0x000000	Reserved
10H	ISUM	R	4	--	Current vector sum RMS
11H	IA_NVM1	R	3	0x000000	Current RMS of phase A in NVM1 mode
12H	IB_NVM1	R	3	0x000000	Current RMS of phase B in NVM1 mode
13H	IC_NVM1	R	3	0x000000	Current RMS of phase C in NVM1 mode

14H	PA	R	4	--	Active power of phase A
15H	PB	R	4	--	Active power of phase B
16H	PC	R	4	--	Active power of phase C
17H	PT	R	4	--	Active power of all-phase
18H	QA	R	4	--	Reactive power of phase A
19H	QB	R	4	--	Reactive power of phase B
1AH	QC	R	4	--	Reactive power of phase C
1BH	QT	R	4	--	Reactive power of all-phase
1CH	SA	R	4	--	Apparent power of phase A
1DH	SB	R	4	--	Apparent power of phase B
1EH	SC	R	4	--	Apparent power of phase C
1FH	ST	R	4	--	Apparent power of all-phase
20H	PfA	R	3	--	Power factor of phase A
21H	PfB	R	3	--	Power factor of phase B
22H	PfC	R	3	--	Power factor of phase C
23H	PfT	R	3	--	Power factor of all-phase
24H	PAFCnt	R/W	3	--	Active fast pulse count of phase A
25H	PBFCnt	R/W	3	--	Active fast pulse count of phase B
26H	PCFCnt	R/W	3	--	Active fast pulse count of phase C
27H	PTFCnt	R/W	3	--	Active fast pulse count of all-phase
28H	QAFCnt	R/W	3	--	Reactive fast pulse count of phase A
29H	QBFCnt	R/W	3	--	Reactive fast pulse count of phase B
2AH	QCFCnt	R/W	3	--	Reactive fast pulse count of phase C
2BH	QTFCnt	R/W	3	--	Reactive fast pulse count of all-phase
2CH	SAFCnt	R/W	3	--	Apparent fast pulse count of phase A

2DH	SBFCnt	R/W	3	--	Apparent fast pulse count of phase B
2EH	SCFCnt	R/W	3	--	Apparent fast pulse count of phase C
2FH	STFCnt	R/W	3	--	Apparent fast pulse count of all-phase
30H	EPA	R	3	--	Active energy register of phase A
31H	EPB	R	3	--	Active energy register of phase B
32H	EPC	R	3	--	Active energy register of phase C
33H	EPT	R	3	--	Active energy register of all-phase
34H	PosEPA	R	3	--	Positive active energy register of phase A
35H	PosEPB	R	3	--	Positive active energy register of phase B
36H	PosEPC	R	3	--	Positive active energy register of phase C
37H	Pos EPT	R	3	--	Positive active energy register of all-phase
38H	NegEPA	R	3	--	Reverse active energy register of phase A
39H	NegEPB	R	3	--	Reverse active energy register of phase B
3AH	NegEPC	R	3	--	Reverse active energy register of phase C
3BH	Neg EPT	R	3	--	Reverse active energy register of all-phase
3CH	EQA	R	3	--	Reactive energy register of phase A
3DH	EQB	R	3	--	Reactive energy register of phase B
3EH	EQC	R	3	--	Reactive energy register of phase C
3FH	EQT	R	3	--	Reactive energy register of all-phase
40H	Pos EQA	R	3	--	Positive reactive energy register of phase A
41H	Pos EQB	R	3	--	Positive reactive energy register of phase B
42H	PosEQC	R	3	--	Positive reactive energy register of phase C
43H	PosEQT	R	3	--	Positive reactive energy register of all-phase
44H	Neg EQA	R	3	--	Reverse reactive energy register of phase A
45H	Neg EQB	R	3	--	Reverse reactive energy register of phase B

46H	Neg EQC	R	3	--	Reverse reactive energy register of phase C
47H	Neg EQT	R	3	--	Reverse reactive energy register of all-phase
48H	ESA	R	3	--	Apparent energy register of phase A
49H	ESB	R	3	--	Apparent energy register of phase B
4AH	ESC	R	3	--	Apparent energy register of phase C
4BH	EST	R	3	--	Apparent energy register of RMS all-phase
4CH	STV	R	4	--	Apparent energy register of PQS all-phase
4DH	PfTV	R	3	--	Power factor register of PQSall-phase
4EH	STFVCnt	R/W	3	--	Apparent fast pulse counting register of PQS all-phase
4FH	ESTV	R	3	--	Apparent energy register of PQS all-pahse sum
Fundamental and Hamonic Measurement Parameter Register					
50H	YUA	R	3	0x000000	Fundamental phase angle register of sampling channel UA
51H	YUB	R	3	--	Fundamental phase angle register of sampling channel UB
52H	YUC	R	3	--	Fundamental phase angle register of sampling channel UC
53H	YIA	R	3	--	Fundamental phase angle register of sampling channel IA
54H	YIB	R	3	--	Fundamental phase angle register of sampling channel IB
55H	YIC	R	3	--	Fundamental phase angle register of sampling channel IC
56H	YIN	R	3	--	Fundamental phase angle register of sampling channel IN
57H	UFreq	R	3	--	Voltage line frequency
58H	FUA	R	4	--	Fundamental Voltage RMS of phase A
59H	FUB	R	4	--	Fundamental Voltage RMS of phase B

5AH	FUC	R	4	--	Fundamental Voltage RMS of phase C
5BH	FIA	R	4	--	Fundamental current RMS of phase A
5CH	FIB	R	4	--	Fundamental current RMS of phase B
5DH	FIC	R	4	--	Fundamental current RMS of phase C
5EH	FPA	R	4	--	Fundamental active power of phase A
5FH	FPB	R	4	--	Fundamental active power of phase B
60H	FPC	R	4	--	Fundamental active power of phase C
61H	FPT	R	4	--	Fundamental active power of all-phase
62H	FQA	R	4	--	Fundamental reactive power of phase A
63H	FQB	R	4	--	Fundamental reactive power of phase B
64H	FQC	R	4	--	Fundamental reactive power of phase C
65H	FQT	R	4	--	Fundamental reactive power of all-phase
66H	FSA	R	4	--	Fundamental apparent power of phase A
67H	FSB	R	4	--	Fundamental apparent power of phase B
68H	FSC	R	4	--	Fundamental apparent power of phase C
69H	FSTA	R	4	--	Fundamental apparent power of all-phase
6AH	FPfA	R	3	--	Fundamental power factor of phase A
6BH	FPfB	R	3	--	Fundamental power factor of phase B
6CH	FPfC	R	3	--	Fundamental power factor of phase C
6DH	FPfTA	R	3	--	Fundamental power factor of all-phase
6EH	FPAFCnt	R/W	3	--	Fundamental active fast pulse count of phase A
6FH	FPBFCnt	R/W	3	--	Fundamental active fast pulse count of phase B
70H	FPCFCnt	R/W	3	--	Fundamental active fast pulse count of phase C
71H	FPTFCnt	R/W	3	--	Fundamental active fast pulse count of all-

					phase
72H	FQAFCnt	R/W	3	--	Fundamental reactive fast pulse count of phase A
73H	FQBFCnt	R/W	3	--	Fundamental reactive fast pulse count of phase B
74H	FQCFCnt	R/W	3	--	Fundamental reactive fast pulse count of phase C
75H	FQTFCnt	R/W	3	--	Fundamental reactive fast pulse count of all-phase
76H	FSAFCnt	R/W	3	--	Fundamental apparent fast pulse count of phase A
77H	FSBFCnt	R/W	3	--	Fundamental apparent fast pulse count of phase B
78H	FSCFCnt	R/W	3	--	Fundamental apparent fast pulse count of phase C
79H	FSTAFCnt	R/W	3	--	Fundamental apparent fast pulse count of all-phase
7AH	FEPA	R	3	--	Fundamental active energy of phase A
7BH	FEPB	R	3	--	Fundamental active energy of phase B
7CH	FEPC	R	3	--	Fundamental active energy of phase C
7DH	FEPT	R	3	--	Fundamental active energy of all-phase
7EH	PosFEPA	R	3	--	Fundamental positive active energy register of phase A
7FH	PosFEPB	R	3	--	Fundamental positive active energy register of phase B
80H	PosFEPC	R	3	--	Fundamental positive active energy register of phase C
81H	PosFEPT	R	3	--	Fundamental positive active energy register of all-phase
82H	NegFEPA	R	3	--	Fundamental reverse active energy register of phase A
83H	NegFEPB	R	3	--	Fundamental reverse active energy register of phase B

84H	NegFEPC	R	3	--	Fundamental reverse active energy register of phase C
85H	Neg FEPT	R	3	--	Fundamental reverse active energy register of all-phase
86H	FEQA	R	3	--	Fundamental reactive energy of phase A
87H	FEQB	R	3	--	Fundamental reactive energy of phase B
88H	FEQC	R	3	--	Fundamental reactive energy of phase C
89H	FEQT	R	3	--	Fundamental reactive energy of all-phase
8AH	PosFEQA	R	3	--	Fundamental positive reactive energy register of phase A
8BH	PosFEQB	R	3	--	Fundamental positive reactive energy register of phase B
8CH	PosFEQC	R	3	--	Fundamental positive reactive energy register of phase C
8DH	Pos FEQT	R	3	--	Fundamental positive reactive energy register of all-phase
8EH	NegFEQA	R	3	--	Fundamental reverse reactive energy register of phase A
8FH	NegFEQB	R	3	--	Fundamental reverse reactive energy register of phase B
90H	NegFEQC	R	3	--	Fundamental reverse reactive energy register of phase C
91H	NegFEQT	R	3	--	Fundamental reverse reactive energy register of all-phase
92H	FESA	R	3	--	Fundamental apparent energy register of phase A
93H	FESB	R	3	--	Fundamental apparent energy register of phase B
94H	FESC	R	3	--	Fundamental apparent energy register of phase C
95H	FESTA	R	3	--	Fundamental apparent energy register of all-phase
96H	HUA	R	4	--	Harmonic voltage RMS of phase A

97H	HUB	R	4	--	Harmonic voltage RMS of phase B
98H	HUC	R	4	--	Harmonic voltage RMS of phase C
99H	HIA	R	4	--	Harmonic current RMS of phase A
9AH	HIB	R	4	--	Harmonic current RMS of phase B
9BH	HIC	R	4	--	Harmonic current RMS of phase C
9CH	FSTV	R	4	--	Fundamental apparent power of PQS all-phase
9DH	FPfTV	R	3	--	Fundamental power factor of PQS all-phase
9EH	FSTVFCnt	R/W	3	--	Fundamental apparent fast pulse counting of PQS all-phase
9FH	FESTV	R	3	--	Fundamental apparent energy register of PQS all-phase
A0H	UA_HW	R	4	--	RMS of A-phase voltage
A1H	UB_HW	R	4	--	RMS of B-phase voltage
A2H	UC_HW	R	4	--	RMS of C-phase voltage
A3H	IA_HW	R	4	--	Half-cycle RMS of A-phase current
A4H	IB_HW	R	4	--	Half-cycle RMS of B-phase current
A5H	IC_HW	R	4	--	Half-cycle RMS of C-phase current
A6H	UAPEAK_HW	R	2	--	Hal-wave peak of A-phase voltage
A7H	UBPEAK_HW	R	2	--	Hal-wave peak of B-phase voltage
A8H	UCPEAK_HW	R	2	--	Hal-wave peak of C-phase voltage
A9H	IN_HW	R	4	--	Half-cycle RMS of null wire current
AAH	FUA_WAVE	R	3	--	Instantaneous fundamental sampling waveform of A-phase voltage
ABH	FUB_WAVE	R	3	--	Instantaneous fundamental sampling waveform of B-phase voltage
ACH	FUC_WA	R	3	--	Instantaneous fundamental sampling

	VE				waveform of C-phase voltage
ADH	FIA_WAVE	R	3	--	Instantaneous fundamental sampling waveform of A-phase current
AEH	FIB_WAVE	R	3	--	Instantaneous fundamental sampling waveform of B-phase current
AFH	FIC_WAVE	R	3	--	Instantaneous fundamental sampling waveform of C-phase current
B0H	FIN_WAVE	R	3	--	Instantaneous fundamental sampling waveform of null wire current
B1H	SPL_PA	R	4	--	Instantaneous active power of A-phase (Half-cycle active power of A-phase)
B2H	SPL_PB	R	4	--	Instantaneous active power of B-phase (Half-cycle active power of B-phase)
B3H	SPL_PC	R	4	--	Instantaneous active power of C-phase (Half-cycle active power of C-phase)
B4H	SPL_QA	R	4	--	Instantaneous reactive power of A-phase (Half-cycle RMS reactive power of A-phase)
B5H	SPL_QB	R	4	--	Instantaneous reactive power of B-phase (Half-cycle RMS reactive power of B-phase)
B6H	SPL_QC	R	4	--	Instantaneous reactive power of C-phase (Half-cycle RMS reactive power of C-phase)
B7H	SPL_FPA	R	4	--	Instantaneous fundamental active power of A-phase (Half fundamental active power of A-phase)
B8H	SPL_FPB	R	4	--	Instantaneous fundamental active power of B-phase (Half fundamental active power of B-phase)

B9H	SPL_FPC	R	4	--	Instantaneous fundamental active power of C-phase (Half fundamental active power of C-phase)
BAH	SPL_FQA	R	4	--	Instantaneous fundamental reactive power of A-phase (Half fundamental reactive power of A-phase)
BBH	SPL_FQB	R	4	--	Instantaneous fundamental reactive power of B-phase (Half fundamental reactive power of B-phase)
BCH	SPL_FQC	R	4	--	Instantaneous fundamental reactive power of C-phase (Half fundamental reactive power of C-phase)
BDH	RMS_LA 1	R	3	--	Loss of voltage measures IA RMS, single update
BEH	RMS_LB 1	R	3	--	Loss of voltage measures IB RMS, single update
BFH	RMS_LC 1	R	3	--	Loss of voltage measures IC RMS, single update
C0H	FLK_UA	R	4	--	Instantaneous voltage of UA channel
C1H	FLK_UB	R	4	--	Instantaneous voltage of UB channel
C2H	FLK_UC	R	4	--	Instantaneous voltage of UC channel
C3H	SAG_UA PEAK	R	2	--	SAG peak min register of UA channel
C4H	SAG_UB PEAK	R	2	--	SAG peak min register of UB channel
C5H	SAG_UC PEAK	R	2	--	SAG peak min register of UC channel
C6H	UA_HW2	R	4	--	Half-cycle RMS voltage 2 of A-phase
C7H	UB_HW2	R	4	--	Half-cycle RMS voltage 2 of B-phase
C8H	UC_HW2	R	4	--	Half-cycle RMS voltage 2 of C-phase
C9H	IA_HW2	R	4	--	Half-cycle RMS current 2 of A-phase
CAH	IB_HW2	R	4	--	Half-cycle RMS current 2 of B-phase

Address	Name	R/W	Byte Length	EMM Power-up Reset	Description
CBH	IC_HW2	R	4	--	Half-cycle RMS current 2 of C-phase
CCH	IN_HW2	R	4	--	Half-cycle RMS current 2 of null wire
CDH	FLK_RSLTA	R	4	--	Flickering register of UA channel
CEH	FLK_RSLTB	R	4	--	Flickering register of UB channel
CFH	FLK_RSLTC	R	4	--	Flickering register of UC channel
F9H	PTFCnt2	R	3	--	Active power fast pulse counting register 2 of all-phase
FAH	QTFCnt2	R	3	--	Reactive power fast pulse counting register 2 of all-phase
FBH	STFCnt2	R	3	--	Apparent power fast pulse counting register 2 of all-phase
FCH	FPTFCnt2	R	3	--	Fundamental active power fast pulse counting register 2 of all-phase
FDH	FQTFCnt2	R	3	--	Fundamental reactive power fast pulse counting register 2 of all-phase
FEH	FSTFCnt2	R	3	--	Fundamental apparent power fast pulse counting register 2 of all-phase

Table 3-1 Parameter Register (Bank6, refer to Section 5.1 for address mappings) List

Address	Name	R/W	Byte Length	EMM Power-up Reset	Description
Total Measurement Parameter Register					
00H	HW_PA	R	4	--	Half-cycle active power of A-phase
01H	HW_PB	R	4	--	Half-cycle active power of B-phase
02H	HW_PC	R	4	--	Half-cycle active power of C-phase
03H	HW_QA	R	4	--	Half-cycle reactive power of A-phase
04H	HW_QB	R	4	--	Half-cycle reactive power of B-phase
05H	HW_QC	R	4	--	Half-cycle reactive power of C-phase

06H	HW_FPA	R	4	--	Fundamental Half-cycle active power of A-phase
07H	HW_FPB	R	4	--	Fundamental Half-cycle active power of B-phase
08H	HW_FPC	R	4	--	Fundamental Half-cycle active power of C-phase
09H	HW_FQA	R	4	--	Fundamental Half-cycle reactive power of A-phase
0AH	HW_FQB	R	4	--	Fundamental Half-cycle reactive power of B-phase
0BH	HW_FQC	R	4	--	Fundamental Half-cycle reactive power of C-phase
0CH	SPL_FIA	R	4	--	Instantaneous fundamental current of A-phase
0DH	SPL_FIB	R	4	--	Instantaneous fundamental current of B-phase
0EH	SPL_FIC	R	4	--	Instantaneous fundamental current of C-phase
0FH	SPL_FUA	R	4	--	Instantaneous fundamental RMS voltage of A-phase
10H	SPL_FUB	R	4	--	Instantaneous fundamental RMS voltage of B-phase
11H	SPL_FUC	R	4	--	Instantaneous fundamental RMS voltage of C-phase

3.2. Description of Parameter Register

3.2.1. Waveform Sample Register

ADDR	00H	01H	02H	03H	04H	05H	06H
REG	UAWAV	UBWAV	UCWAV	IAWAV	IBWAV	ICWAV	INWAV

The seven ADCs sampled data of MKE304T is output to the waveform sample register after the high-pass filter.

The waveform sample register is a 24-bit signed number and takes the complement code format with the MSB as a sign bit. The data refresh rate is 8KHZ. The data source is the data of the ADC after phase calibration/gain calibration/high-pass filtering.

Assuming that the external input peak is an AC signal with a = 0.1v peak, the value of the waveform sampling register is:

A*0.5*2^23=419430(DEC)=24'H66666(HEX)

When the channel gain is calibrated, the normalized value of the peak for the waveform sample register = Normalized value of corresponding total RMS register * sqrt(2) * 0.5.

For the details on the channel U and the channel I gain calibration, refer to Chapter 4 Calibration.

The flag bit of the flag register WAVUPIF (EMMIF.0) will be set to 1 when the waveform sample register is updated, cleared after write 1 to .If enable the waveform register update interrupt WAVUPIE (EMMIE.0), it will cause the interrupt once the update takes place, and the INTN pin outputs the low level.

3.2.2.RMS Register

ADDR	07H	08H	09H	0AH	0BH	0CH	0DH
REG	UA	UB	UC	USUM/FIN	IA	IB	IC
ADDR	0EH	10H	11H	12H	13H		
REG	IN/FIN	ISUM	IA_NVM1	IB_NVM1	IC_NVM1		
ADDR	58H	59H	5AH	5BH	5CH	5DH	
REG	FUA	FUB	FUC	FIA	FIB	FIC	
ADDR	96H	97H	98H	99H	9AH	9BH	
REG	HUA	HUB	HUC	HIA	HIB	HIC	
ADDR	BDH	BEH	BFH				
REG	RMS_LA1	RMS_LB1	RMS_LC1				

There are six types of RMS registers as follows:

      1 Total voltage RMS and current RMS (UA/UB/UC/IA/IB/IC/IN)

      2 Fundamental voltage RMS and current RMS (FUA/FUB/FUC/FIA/FIB/FIC)

      3 Harmonic voltage RMS and current RMS (HUA/HUB/HUC/HIA/HIB/HIC)

      4 Total voltage and current vector sum voltage RMS and current RMS (USUM/ISUM)

      5 NVM1 current RMS (IA_NVM1/IB_NVM1/IC_NVM1)

      6 A single update of NVM1 RMS current (RMS_LA1/ RMS_LB1/ RMS_LC1)

The type 1-4 of RMS is the four-byte register, which is a 28-bit (bit0-bit27) signed number and takes the complement code format. The bit27 is the sign bit, and bit28-bit31 and bit27 are identical and are always 0.The update cycle of these four types of RMS parameters is 250ms. The null channel fundamental RMS FIN, which shares the address with USUM or IN, allows the USUM or IN register to store the FIN value output through the metering unit configuration register EMUCFG3.

The 4 class of total voltage and current vector sum voltage RMS and current RMS, and the equation is to prevent register overflow

$$USUM = \frac{1}{4} * \sqrt{\frac{1}{T} * \int_0^t (u_A(t) + (u_B(t) + (u_C(t))^2}\, dt;$$

$$ISUM = \frac{1}{4} * \sqrt{\frac{1}{T} * \int_0^t (I_A(t) + (I_B(t) + (I_C(t))^2 \, dt} \ .$$

It is a quarter of the theoretical vector and register, and the application needs to be multiplied by 4 to convert to the theoretical vector sum.

The class 5/6 NVM1 current RMSs are three-byte signed numbers, in complement form, bit23 is the sign bit, bit23 is always zero. Without channel gain calibration, the relationship to the normal metered RMS register should be:

$IA_{NVM1}*(1+GSIA) = IA*0.87909/16$.

The class 6 NVM1 RMS current NVM1 is completed after the calculation time of the LS_THOA configuration is completed. NVM1Done flag position 1 is updated at the same time. Reading the NVM1IF.NVM1Done flag clears zero, which does not clear the RMS_Lx1 calculation, and the RMS_Lx1 registers are retained until the next time the NVM1 detection process is started.

The class 1-4 valid values are valid only under EMM and not under NVM1. Class 5 NVM1 RMS current can be read in both EMM mode and NVM1 mode; Class 6 NVM1 RMS current is valid only in NVM1 mode and reads 0 in EMM mode. Under SLM and NVM2, neither of the above registers is valid.

For the RMS parameters, *the actual voltage and current RMS =KRMSx*RMSReg'*

where KRMSx represents the conversion coefficient and RMSReg' represents the complement of the RMS register above. This operation is done by the MCU.

3.2.3.Half-cycle RMS Register

ADDR	A0H	A1H	A2H	A3H	A4H	A5H	A9H
REG	UA_HW	UB_HW	UC_HW	IA_HW	IB_HW	IC_HW	IN_HW
ADDR	C6H	C7H	C8H	C9H	CAH	CBH	CCH
REG	UA_HW2	UB_HW2	UC_HW2	IA_HW2	IB_HW2	IC_HW2	IN_HW2

Two sets of UA/UB/UC/IA/IB/IC/IN 7-way half-cycle RMS registers, metering channel half-cycle RMS registers and simultaneous sampling half-cycle RMS 2 are provided.

1. Measurement Channel Half-cycle RMS Register

The measurement channel half-cycle RMS register is the sum of squares or RMS of the sampling points in each channel's half-cycle, and the properties of the output result of the metering channel half-cycle RMS register are determined by configuring the RMS_HW_SQRT bits in the metering unit configuration register 2 EMU_CFG2 (B1 0x9A[0]):

=1: The 32-bit half-cycle RMS register represents the result of the open root, with the lower 24 bits valid and the upper 8 bits fixed at 0.

=0: The 32-bit half-cycle RMS register represents the result after the original waveform is squared, 32-bit valid, and a software root-on number is required to obtain the half-cycle RMS.

The half-cycle RMS register is a four-byte unsigned number, and the relationship to the RMS register is discussed below. Half-cycle RMS register parameters are updated half-cycle.

After the user software reads the half-cycle RMS register, it needs to do the square root operation to obtain the complete half-cycle RMS. Take phase A voltage as an example:

$$UA\_HW=K\_UAhw*sqrt(reg (UA\_HW))$$

Where:

UA_HW is phase A voltage half RMS, which is affected by channel gain register GSUA;

reg(UA_HW) is the UA half-cycle RMS register after GSUA register gain calibration, if the RMS A-phase voltage is corrected, no additional gain calibration is required UA_HW;

sqrt is the square root operation, which is done by software;

K_UAhw is transform coefficient, which convert the test values into display values, completed by software.

If the result after the root opening is selected, then the relationship between the half-cycle RMS register HW and the RMS register RMS (0x7~0xE) is:

$$RMS = HW*256/sqrt(4000/Ufreq)$$, where Ufreq is fundamental frequency.

Example: If the half-cycle RMS register HW (selected as the open root) equals 32'h11E090 = decimal 1171600 and the frequency is 50Hz, then the RMS register is:

$$RMS = 1171600*256/sqrt(80) = 299929600/8.94427191 = 33533148.7$$, convert to hexadecimal is: 28'h1FFACDC.

If the result without the root opening sign is chosen, then the relationship between the half-cycle RMS register HW (multiply squared and accumulate) and the RMS register (0x31C~0x338) is

$$RMS = sqrt(HW*2^{16})*256/sqrt(4000/Ufreq)$$, where Ufreq is fundamental frequency.

2．Simultaneous Sampling Channel Half-cycle RMS 2

Synchronous sampling channel half-cycle RMS register 2 is a four-byte unsigned number, 27 bits valid, 5 bits high complement 0. The relationship to the valid value register is described below. The half-cycle RMS register parameter is updated based on the number of HWCNT register set points.

The half-cycle RMS register 2 outputs the result after the square of the set point number and the open root number, then the relationship between the half-cycle RMS register 2HW2 and the RMS register RMS (0x7~0xE) is:

$$RMS = HW2*32/sqrt(N)$$, where N = HWCNT + 1.

Example: If the half-cycle RMS register HW2 is equal to 32'h11E090=decimal 1171600, and the square accumulation point is set to HWCNT=127, then the RMS register is:

$$RMS = 1171600*32/sqrt(128) = 37491200/11.31370850 = 3313785.22$$, convert to hexadecimal is: 22'h329079.

3.2.4.Instantaneous Fundamental RMS Register

ADDR	0CH	0DH	0EH
REG	SPL_FIA	SPL_FIB	SPL_FIC
ADDR	0FH	10H	11H
REG	SPL_FUA	SPL_FUB	SPL_FUC

This type of register is the BANK3 address range register which up to 8 kSPS, its base address is 0x600. Length: 4 bytes, bit31~bit27 are always 0, a total of 27 significant bits.

3.2.5.Average Power Register

ADDR	14H	15H	16H	17H	18H	19H	1AH	1BH
REG	PA	PB	PC	PT	QA	QB	QC	QT
ADDR	1CH	1DH	1EH	1FH	4CH			

REG	SA	SB	SC	STA	STV			
ADDR	5EH	5FH	60H	61H	62H	63H	64H	65H
REG	FPA	FPB	FPC	FPT	FQA	FQB	FQC	FQT
ADDR	66H	67H	68H	69H	9CH			
REG	FSA	FSB	FSC	FSTA	FSTV			

The power registers include total per-phase, all-phase active power PA/PB/PC/PT, reactive power QA/QB/QC/QT, per-phase apparent power SA/SB/SC, all-phase apparent RMS power STA, all-phase apparent PQS power STV; Fundamental per-phase and all-phase active power FPA/FPB/FPC/FPT, reactive power FQA/FQB/FQC/FQT, per-phase apparent power FSA/FSB/FSC, all-phase apparent RMS power FSTA, all-phase apparent PQS power FSTV.

The power registers are in twos complement format with 32 bits with signed numbers, where the highest bit is the sign bit. For apparent power, the highest bit is always 0. The power parameter update period is 250ms。

For the power parameters: actual power = *Kpx* PReg'*

where Kpx represents the conversion factor and PReg' represents the complement of the corresponding power register PReg. This operation is done by the MCU.

3.2.6.Half-cycle Update Power Register

ADDR	00H	01H	02H	03H	04H	05H
REG	HW_PA	HW_PB	HW_PC	HW_QA	HW_QB	HW_QC
ADDR	06H	07H	08H	09H	0AH	0BH
REG	HW_FPA	HW_FPB	HW_FPC	HW_FQA	HW_FQB	HW_FQC

The half-cycle updated power register has an update period of 10ms, including a per-phase total active power register with half-cycle update, a per-phase total reactive power register with half-cycle update, a per-phase fundamental reactive power register with half-cycle update, and a per-phase fundamental active power register with half-cycle update.

Note: This register is in the BANK6 address space, that is, the address base address is 0x00.

3.2.7.Instantaneous Power Register

ADDR	B1H	B2H	B3H	B4H	B5H	B6H
REG	SPL_PA	SPL_PB	SPL_PC	SPL_QA	SPL_QB	SPL_QC
ADDR	B7H	B8H	B9H	BAH	BBH	BCH
REG	SPL_FPA	SPL_FPB	SPL_FPC	SPL_FQA	SPL_FQB	SPL_FQC

The instantaneous power register update speed is 8Khz, including per-phase active power, per-phase reactive power, and per-phase fundamental active power, per-phase fundamental reactive power. The calculation formula is the same as the average power register.

Example: Assuming that the voltage channel input is a sine wave with a peak of 0.35mV and the current channel input is a sine wave with a peak of 0.05mV, and the phase between the two is 0 degrees, then the power register is approximate:

PowerP=0.35*0.05*0.5*2^31=18790481 (DEC) =11EB851 (HEX)

3.2.8.Power Factor Register

ADDR	20H	21H	22H	23H	4DH	6AH	6BH	6CH
REG	PfA	PfB	PfC	PfTA	PfTV	FPfA	FPfB	FPfC
ADDR	6DH	9DH						
REG	FPfTA	FPfTV						

The power factor register includes total per-phase power factor PfA/PfB/PfC, all-phase RMS power factor PfTA, all-phase PQS power factor PfTV; Fundamental per-phase power factor FPfA/FPfB/FPfC, all-phase RMS power factor FPfTA, all-phase PQS power factor FPfTV.

The power factor register uses twos complement format with 24 bits of signed numbers, where the highest bit is the sign bit, determined by the active power sign bit. The power factor parameter update period is 250ms.

Power factor parameter calculation formula: *Actual power factor= PfReg'/2^{23}*

where PfReg' represents the complement of the corresponding power factor register, PfReg.

3.2.9.Fast Pulse Counting Register

ADDR	24H	25H	26H	27H	28H	29H	2AH
REG	PAFCnt	PBFCnt	PCFCnt	PTFCnt	QAFCnt	QBFCnt	QCFCnt
ADDR	2BH	2CH	2DH	2EH	2FH	4EH	
REG	QTFCnt	SAFCnt	SBFCnt	SCFCnt	STFACnt	STFVCnt	
ADDR	6EH	6FH	70H	71H	72H	73H	74H
REG	FPAFCnt	FPBFCnt	FPCFCnt	FPTFCnt	FQAFCnt	FQBFCnt	FQCFCnt
ADDR	75H	76H	77H	78H	79H	9EH	
REG	FQTFCnt	FSAFCnt	FSBFCnt	FSCFCnt	FSTFACnt	FSTVFCnt	
ADDR	F9H	FAH	FBH	FCH	FDH	FEH	
REG	PTFCnt2	QTFCnt2	STFCnt2	FPTFCnt2	FQTFCnt2	FSTFCnt2	

Fast pulse counting register includes total/fundamental, active/reactive/apparent registers, per-phase/all-phase fast pulse counting registers。

The fast pulse count register is an 18-bit (bit0-bit17) signed number, where bit17 is the sign bit, determined by the power sign bit, and bit18-bit23 is an invalid bit and fixed at 0.

Fast pulse counting can be configured through EMUCFG2.bit27~bit4 registers, and four phase-accumulate modes are as follows:

1. Algebraic sum and additive mode: when the input is positive, Fcnt is positive, HFCONST1 and Fcnt/2 are compared, equal, Fcnt is cleared, and the corresponding energy register is increased by 1. When the input is reversed, the negative direction of Fcnt increases, the complement of HFCONST1 and Fcnt/2 is compared, equal, Fcnt is cleared, and the corresponding energy register is increased by 1.

2. Absolute accumulation mode: PXFCnt pair|PX|Integrated, compared with the corresponding HFConst, EPX increases by 1 and CF outputs pulses. In this mode, PXFCnt is always positive, EPX=PosEPX, NegEPX=0.

3. Positive accumulation mode: PXFCnt integrates only at PX≥0, and after comparison with the corresponding HFConst, the EPX is increased by 1 and the CF output pulse is output. In this mode, PXFCnt is always positive, EPX=PosEPX, and NegEPX is negative active energy.

4. Negative accumulation mode: In this mode, only integration at PX<0, after comparison with the corresponding HFConst, EPX increases by 1 and CF outputs a pulse. In this mode, PXFCnt is always negative, EPX=NegEPX, and PosEPX is the positive active energy.

The default is algebraic sum and additive modes, and each phase active/reactive mode of fundamental and total can be configured separately.

When WREN write is enabled, the fast pulse counting register is writable, and the write value is readable and writable when the absolute of 18 bits is less than HFCONST1*2, and the write is invalid when greater than or equal to HFCONST1*2.

Registers such as PTFCnt2 are conjunction fast pulse counting registers (3-byte registers) independently configured by HFCONST2, which are 18 bits (bit0-bit17) signed numbers, where bit17 is the sign bit, determined by the power sign bit, bit18-bit23 is an invalid bit, fixed at 0.

When the input is positive, the Fcnt positive direction increases, HFCONST2 and Fcnt/2 are compared, equal, Fcnt is cleared, and 1 corresponding pulse is output. When the input is reversed, the negative direction of Fcnt increases, the complement of HFCONST2 and Fcnt/2 is compared, equal, Fcnt is cleared, and 1 corresponding pulse is output.

When WREN2 write is enabled, the conjoined fast pulse count register independently configured by HFCONST2 is writable, and the write value is readable and writable when the absolute of 18 bits is less than HFCONST2*2, and the write is invalid when it is greater than or equal to HFCONST2*2.

3.2.10.Energy Register

ADDR	30H	31H	32H	33H	34H	35H	36H
REG	EPA	EPB	EPC	EPT	PosEPA	PosEPB	PosEPC
ADDR	37H	38H	39H	3AH	3BH	3CH	3DH
REG	PosEPT	NegEPA	NegEPB	NegEPC	NegEPT	EQA	EQB
ADDR	3EH	3FH	40H	41H	42H	43H	44H
REG	EQC	EQT	PosEQA	PosEQB	PosEQC	PosEQT	NegEQA
ADDR	45H	46H	47H	48H	49H	4AH	4BH
REG	NegEQB	NegEQC	NegEQT	ESA	ESB	ESC	ESTA
ADDR	4FH	7AH	7BH	7CH	7DH	7EH	7FH
REG	ESTV	FEPA	FEPB	FEPC	FEPT	PosFEPA	PosFEPB

ADDR	80H	81H	82H	83H	84H	85H	86H
REG	PosFEPC	PosFEPT	NegFEPA	NegFEPB	NegFEPC	NegFEPT	FEQA
ADDR	87H	88H	89H	8AH	8BH	8CH	8DH
REG	FEQB	FEQC	FEQT	PosFEQA	PosFEQB	PosFEQC	PosFEQT
ADDR	8EH	8FH	90H	91H	92H	93H	94H
REG	NegFEQA	NegFEQB	NegFEQC	NegFEQT	FESA	FESB	FESC
ADDR	95H	9FH					
REG	FESTA	FESTV					

The energy register is a 24-bit unsigned number. The smallest unit of register represents the energy of 1/EC KWh, where EC is the meter constant.

The chip have several types of energy registers, including fundamental/total , active/reactive/apparent phase, per/conjunction, active, and reactive positive/reverse energy registers.

The energy register can be configured as either zero-clear or additive. Register bit ERegCAR(EMUCFG.19)=0, all energy registers are zero-cleared; =1, which is additive. The default is reset.

Positive active and reactive energy registers only measure electrical energy with a power greater than 0; The reverse active and reactive energy registers only measure energy with a power less than 0.

In three-phase four-wire mode, the accumulation mode of the conjunct functional quantity register can be configured as either algebraic sum or absolute sum, positive accumulation sum, negative accumulation and type. Register bits {EPADDMODE1(EMUCFG.8), EPADDMODE0(EMUCFG.20)} = 2'b00, the accumulation mode is algebraic sum type, and the conjunction has the power of the algebra and PA+PB+PC integral;

=2'b01, is the absolute sum type. The all-phase active energy is obtained by de integrating the sum of the absolutes of the per-phase power |PA|+|PB|+|PC|;

=2'b10, is the positive accumulation and sum type. The all-phase reactive energy is only integrated in the positive direction;

=2'b11, is the negative accumulation sum type. The all-phase reactive energy is only integrated in the negative direction;

The default is algebraic sum type.

In three-phase four-wire mode, the accumulation mode of the all-phase non-functional quantity register can be configured as either algebraic sum or absolute sum, positive accumulation sum, negative accumulation and type. Register bits {EQADDMODE1(EMUCFG.9), EQADDMODE0(EMUCFG.21)}=2'b00, the accumulation mode is algebraic sum type, the conjunction has no functional quantity in the algebra of the per phase power and QA+QB+QC integral;

=2'b01, is the absolute sum type. The all-phase active energy is obtained by de integrating the sum of the absolutes of the per-phase power |QA|+|QB|+|QC|;

=2'b10, is the positive accumulation and sum type. The all-phase reactive energy is only integrated in the positive direction;

=2'b11, is the negative accumulation sum type. The all-phase reactive energy is only integrated in the negative direction;

The default is algebraic sum type.

Note that the accumulation mode of the active and reactive all-phase energy registers works only for the all-phase energy register, not the all-phase power register.

In three-phase three-wire mode, the combined active and non-functional registers are only algebraic sum types. Register bits EPADDMODE, EQADDMODE are not configurable.

3.2.11.Phase Angle Register

ADDR	50H	51H	52H	53H	54H	55H	56H
REG	YUA	YUB	YUC	YIA	YIB	YIC	YIN

These registers are 24-bit unsigned number, which indicates the phase angle for each sample channel fundamental and the reference voltage channel fundamental. If take the UA channel as the phase angle reference, YIB indicates the phase angle between the fundamental IB and the fundamental UA. Users can get the phase angle of any two phases by the simple operation, for example, the phase angle between IA and IB is YIAIB = YIA - YIB. The update cycle is 32 signal cycles.

Three-phase four-wire: If FUA>ZXOT (normalized value, the same below), take the UA channel as the phase angle test benchmark. If FUA <ZXOT and FUB > ZXOT, take the UB channel as the phase angle test benchmark. If FUA<ZXOT, FUB<ZXOT and FUC>ZXOT, take the UC channel as the phase angle test benchmark. If three phase fundamental voltages< ZXOT, each phase angles are 0.

Three-phase three-wire: If FUA > ZXOT, take the UA channel as the phase angle test benchmark. If FUA<ZXOT and FUC > ZXOT, take the UC channel as the phase angle test benchmark. If both FUA and FUC < ZXOT, each phase angles are 0.

When take the UA channel as the benchmark, if any one of FUB, FUC, FIA, FIB, FIC and FIN< ZXOT, this phase angle is 0, and if any one of FUC, FIA, FIB, FIC and FIN<ZXOT, this phase angle is 0. When take the UC channel as the benchmark, if any one of FIA, FIB, FIC and FIN< ZXOT, this phase angle is 0

Calculation Formula of Phase Angle: Actual Phase Angle = (REGY/224)*360°. REGY indicates the value of the phase angle register.

3.2.12.Voltage Line Frequency Register

ADDR: 57H; REG: UFreq

This register is a 24-bit unsigned number, is the line frequency of the voltage. The update period of the line frequency register can be selected as one-cycle or 32-cycle by registering the 21-bit Freq_Cycle of the EMUCFG3.

Three-phase four-wire: If FUA > ZXOT (normalized value, the same below), take the UA channel as the frequency test benchmark. If FUA<ZXOT and FUB > ZXOT, take the UB channel as the frequency test benchmark. If FUA<ZXOT, FUB<ZXOT and FUC > ZXOT, take the UC channel as the frequency test benchmark.

Three-phase three-wire: If FUA > ZXOT, take the UA channel as the frequency test benchmark. If FUA<ZXOT and FUC > ZXOT, take the UC channel as the frequency test benchmark.

Calculation Formula of Voltage Line Frequency: Actual Frequency = fosc*8/REGF. REGF indicates the value of the frequency register.

3.2.13.SAG Peak Min Register

ADDR	C3H	C4H	C5H
REG	SAG_UAPEAK	SAG_UBPEAK	SAG_UCPEAK

The SAG peak minimum register records the set time (SAGCFG. SAGCYC[7:0]--Bank1 0x58) The upper 16 bits of the lowest of the absolutes of all half-cycle peaks of all voltages in a phase. The significant digits are [15: 0], which is a 16-bit unsigned number.

3.2.14.Half-peak Voltage Register

ADDR	A6H	A7H	A8H
REG	UAPEAK_HW	UBPEAK_HW	UCPEAK_HW

The voltage half-cycle peak register is the upper 16 bits of the absolute half-cycle peak of a phase voltage wa veform 8K sampling. The significant digits are [15:0], which is a 16-bit unsigned number.

Conversion relationship with valid values, using UA as an example:

$UAPEAK\_HW/2^{16}/Sqrt(2) = 0.5*UA/2^{27}$，

When the internal overvoltage is determined, this register is compared to the OVLVL [15:0] threshold.

Relevant register: Voltage channel gain register GSUx.

3.2.15.Flickering Register

ADDR	C0H	C1H	C2H
REG	FLK_UA	FLK_UB	FLK_UC
ADDR	CDH	CEH	CFH
REG	FLK_RSLTA	FLK_RSLTB	FLK_RSLTC

The registers FLK_UA_, FLK_UB, and FLK_UC represent 20-byte FIFOs per channel, storing 5 instantaneous samplings within 10ms, and instantaneous samplings are updated at 500Hz;

The registers FLK_RSLTA, FLK_RSLTB, and FLK_RSLTC store 1 flicker calculation result, the upper 12 bits of each calculation result are integers, the lower 20 bits are decimals, and the actual value can be obtained by dividing by 2^{20} when calculating.

3.3.Configuration and Status Register List

Table 3-2 Configuration and Status Register (Bank1, address mapping refer to Section 5.1) List

Address	Name	R/W	Byte Length	EMM Power-up Reset	Description
EMM Calibration Register					
00H	HFConst1	R/W	2	0x1000	High-frequency pulse constant register 1
01H	HFConst2	R/W	2	0x1000	High-frequency pulse constant register 2
02H	IStart_PS	R/W	2	0x0250	Active and apparent startup current threshold register
03H	IStart_Q	R/W	2	0x0250	Reactive startup current threshold register
04H	LostVoltT	R/W	2	0x0400	Loss of voltage threshold
05H	ZXOT	R/W	2	0x0073	Zero-crossing threshold

06H	PRTH1L	R/W	2	0x0000	Lower limit of segment phase calibration current threshold 1
07H	PRTH1H	R/W	2	0x0000	Upper limit of segment phase calibration current threshold 1
08H	PRTH2L	R/W	2	0x0000	Lower limit of segment phase calibration current threshold 2
09H	PRTH2H	R/W	2	0x0000	Upper limit of segment phase calibration current threshold 2
0AH	IRegion3L	R/W	2	0x0000	Lower limit of current threshold 3
0BH	IRegion3H	R/W	2	0x0000	Upper limit of current threshold 3
0CH	PHSUA	R/W	1	0x80	Phase calibration register of sampling channel UA
0DH	PHSUB	R/W	1	0x80	Phase calibration register of sampling channel UB
0EH	PHSUC	R/W	1	0x80	Phase calibration register of sampling channel UC
0FH	PHSIA	R/W	3	0x808080	Per-phase calibration register of sampling channel IA
10H	PHSIB	R/W	3	0x808080	Per-phase calibration register of sampling channel IB
11H	PHSIC	R/W	3	0x808080	Per-phase calibration register of sampling channel IC
12H	PHSIN	R/W	1	0x80	Phase calibration of sample channel IN
13H	GSUA	R/W	2	0x0000	Channel gain of sample channel UA
14H	GSUB	R/W	2	0x0000	Channel gain of sample channel UB
15H	GSUC	R/W	2	0x0000	Channel gain of sample channel UC
16H	GSIA	R/W	2	0x0000	Channel gain of sample channel IA
17H	GSIB	R/W	2	0x0000	Channel gain of sample channel IB
18H	GSIC	R/W	2	0x0000	Channel gain of sample channel IC
19H	GSIN	R/W	2	0x0000	Channel gain of sample channel IN
1AH	DCOS_UA	R/W	2	0x0000	DC OFFSET calibration of sample channel UA
1BH	DCOS_UB	R/W	2	0x0000	DC OFFSET calibration of sample channel UB

1CH	DCOS_UC	R/W	2	0x0000	DC OFFSET calibration of sample channel UC
1DH	DCOS_IA	R/W	2	0x0000	DC OFFSET calibration of sample channel IA
1EH	DCOS_IB	R/W	2	0x0000	DC OFFSET calibration of sample channel IB
1FH	DCOS_IC	R/W	2	0x0000	DC OFFSET calibration of sample channel IC
20H	DCOS_IN	R/W	2	0x0000	DC OFFSET calibration of sample channel IN
21H	UA_OS	R/W	2	0x0000	Voltage RMS Offset of phase A
22H	UB_OS	R/W	2	0x0000	Voltage RMS Offset of phase B
23H	UC_OS	R/W	2	0x0000	Voltage RMS Offset of phase C
24H	IA_OS	R/W	2	0x0000	Current RMS Offset of phase A
25H	IB_OS	R/W	2	0x0000	Current RMS Offset of phase B
26H	IC_OS	R/W	2	0x0000	Current RMS Offset of phase C
27H	IN_OS	R/W	2	0x0000	Current RMS Offset of null line 1
28H	GPA	R/W	2	0x0000	Active power gain of phase A
29H	GPB	R/W	2	0x0000	Active power gain of phase B
2AH	GPC	R/W	2	0x0000	Active power gain of phase C
2BH	GQA	R/W	2	0x0000	Reactive power gain of phase A
2CH	GQB	R/W	2	0x0000	Reactive power gain of phase B
2DH	GQC	R/W	2	0x0000	Reactive power gain of phase C
2EH	GSA	R/W	2	0x0000	Apparent power gain of phase A
2FH	GSB	R/W	2	0x0000	Apparent power gain of phase B
30H	GSC	R/W	2	0x0000	Apparent power gain of phase C
31H	PA_PHS	R/W	2	0x0000	Active phase calibration register of phase A
32H	PB_PHS	R/W	2	0x0000	Active phase calibration register of phase B
33H	PC_PHS	R/W	2	0x0000	Active phase calibration register of phase C
34H	QA_PHS	R/W	2	0x0000	Reactive phase calibration register of phase A

35H	QB_PHS	R/W	2	0x0000	Reactive phase calibration register of phase B
36H	QC_PHS	R/W	2	0x0000	Reactive phase calibration register of phase C
37H	PA_OS	R/W	2	0x0000	Active power Offset of phase A
38H	PB_OS	R/W	2	0x0000	Active power offset of phase B
39H	PC_OS	R/W	2	0x0000	Active power offset of phase C
3AH	QA_OS	R/W	2	0x0000	Reactive power offset of phase A
3BH	QB_OS	R/W	2	0x0000	Reactive power offset of phase B
3CH	QC_OS	R/W	2	0x0000	Reactive power offset of phase C
3DH	FUA_OS	R/W	2	0x0000	Fundamental voltage RMS offset of phase A
3EH	FUB_OS	R/W	2	0x0000	Fundamental voltage RMS offset of phase B
3FH	FUC_OS	R/W	2	0x0000	Fundamental voltage RMS offset of phase C
40H	FIA_OS	R/W	2	0x0000	Fundamental current RMS offset of phase A
41H	FIB_OS	R/W	2	0x0000	Fundamental current RMS offset of phase B
42H	FIC_OS	R/W	2	0x0000	Fundamental current RMS offset of phase C
43H	GFPA	R/W	2	0x0000	Fundamental active power gain of phase A
44H	GFPB	R/W	2	0x0000	Fundamental active power gain of phase B
45H	GFPC	R/W	2	0x0000	Fundamental active power gain of phase C
46H	GFQA	R/W	2	0x0000	Fundamental reactive power gain of phase A
47H	GFQB	R/W	2	0x0000	Fundamental reactive power gain of phase B
48H	GFQC	R/W	2	0x0000	Fundamental reactive power gain of phase C
49H	GFSA	R/W	2	0x0000	Fundamental apparent power gain of phase A
4AH	GFSB	R/W	2	0x0000	Fundamental apparent power gain of phase B
4BH	GFSC	R/W	2	0x0000	Fundamental apparent power gain of phase C
4CH	FPA_PHS	R/W	2	0x0000	Fundamental active phase calibration register of phase A
4DH	FPB_PHS	R/W	2	0x0000	Fundamental active phase calibration register of

					phase B
4EH	FPC_PHS	R/W	2	0x0000	Fundamental active phase calibration register of phase C
4FH	FQA_PHS	R/W	2	0x0000	Fundamental reactive phase calibration register of phase A
50H	FQB_PHS	R/W	2	0x0000	Fundamental reactive phase calibration register of phase B
51H	FQC_PHS	R/W	2	0x0000	Fundamental reactive phase calibration register of phase C
52H	FPA_OS	R/W	2	0x0000	Fundamental active power offset of phase A
53H	FPB_OS	R/W	2	0x0000	Fundamental active power offset of phase B
54H	FPC_OS	R/W	2	0x0000	Fundamental active power offset of phase C
55H	FQA_OS	R/W	2	0x0000	Fundamental reactive power offset of phase A
56H	FQB_OS	R/W	2	0x0000	Fundamental reactive power offset of phase B
57H	FQC_OS	R/W	2	0x0000	Fundamental reactive power offset of phase C
58H	SAGCFG	R/W	3	0x000000	Voltage sag threshold configuration
59H	OVLVL	R/W	2	0x0000	Overvoltage threshold configuration
5AH	OILVL	R/W	2	0x0000	Overcurrent threshold configuration
5BH	ISUM_OS	R/W	2	0x0000	Current vector and OFFSET calibration register
5CH	HFConst0	R/W	2	0x0000	High frequency pulse counting register 0
5DH	TTEEC_EN	R/W	1	0x00	Three-phase three-wire error wiring metering calibration enable register
5EH	UCHSEL	R/W	1	0x00	Voltage channel select register
EMM Configuration and Status Register					
60H	CFCFG	R/W	3	0x043210	CF pin configuration register
61H	EMUCFG	R/W	3	0x400000	EMU configuration register
9AH	EMUCFG2	R/W	4	0x4	EMU configuration register 2
62H	EMUCON	R/W	3	0x000000	EMU control register

63H	WSAVECON	R/W	1	0x00	Sampling data write buffer control register
64H	EMMIE	R/W	2	0x0000	EMM interrupt enable register, write protection
65H	EMMIF	R	2	--	EMM interrupt flag and status register
66H	PQSign	R	2	--	Active and reactive power orientation register
67H	Noload	R	2	--	No-load and startup status register
68H	IRegionS	R	1	--	Current segment status register
69H	PHASES	R	2	--	Phase voltage and current status register
6AH	CheckSum1	R	3	--	EMM calibration and configuration register checksum
6BH	EMMIE2	R/W	4	0x0	EMM interrupt enable register
6CH	EMMIF2	R/W	4	--	EMM interrupt flag and status register
6DH	EMUCFG3	R/W	4	0x0	EMU configuration register 3
6EH	EMUCFG4	R/W	4	0x0	EMU configuration register 4
6FH	SPECFG	R/W	4	0x0	EMU special function configuration register
NVM1 Configuration and Status Register					
70H	NVM1CFG	R/W	1	0x01	NVM1 configuration register
71H	NVM1IF	R	1	--	NVM1 status register
NVM2 Configuration and Status Register					
72H	NVM2CFG	R/W	2	0x0F21	NVM2 Configuration Register
73H	NVM2CMPA	R/W	2	0x0256	NVM2 IA comparator control register
74H	NVM2CMPB	R/W	2	0x0256	NVM2 IB comparator control register
75H	NVM2CMPC	R/W	2	0x0256	NVM2 IC comparator control register
76H	NVM2IF	R	1	0x00	NVM2 status register
System Configuration Register					
78H	SYSCFG	R/W	4	0x38A00	System configuration register
79H~	Reserved				Reserved

7EH					
7FH	WREN2	R/W	4	--	Writer enable register 2
80H	WREN	R/W	1	0x00	Write enable register
81H	WMSW	R/W	1	It is the same as the pin PM configuration.	Operating mode switching register
82H	SOFTRST	R/W	1	0x00	Software reset register
83H	ADCCFG	R/W	2	0x0000	ADC configuration register
84H	TFEEC_EN	R/W	1	0x00	Polyphase, four-wire error wiring metering calibration enable register
85H	ICHSEL	R/W	1	0x00	Current channel select register
86H	MODSEL	R/W	1	0x00	Three-phase four-wire/three-phase three-wire mode selection register
System Status Register					
8AH	SYSSR	R	2	--	System status register
8BH	CheckSum2	R	2	--	NVM1, NVM2 system configuration register checksum
8CH	Reserved			--	Data read by SPI previous time
8DH	WData	R	3/4	--	Data written by SPI previous time
8EH	LRBufAddr	R	2	0x0000	Address of waveform buffer read last time
8FH	DeviceID	R	3	0x830200	MKE304T Device ID
EMM calibration register II					
90H	ZXOTU	R/W	2	0x0000	Voltage angle and frequency measurement threshold registers
91H	AUOTDC_EN	R/W	2	0x0000	DC OFFSET automatic calibration of enable registers
92H	ZXOTCFG	R/W	2	0x0000	Zero-crossing calculation configuration and flag register, double-byte, is actually valid as 12 bits. Zxotcfg[11:5], read only. Store the angle calculation flag bits of each channel, 1 indicates that the channel participates in the angle calculation; 0 means not

					participating, the angle register is read out as 0, and the order is {IN/IC/IB/IA/UC/UB/UA}.
					Zxotcfg[4:0], read and write;
					Zxotcfg[4]: =1.The voltage angle and frequency measurement calculation threshold are selected as ZXOTU; =0. The voltage angle and frequency measurement calculation threshold are selected as ZXOT.
					Zxotcfg[3]: =1. When there are three phases and three wires, the voltage of B mode participates in the calculation of the angle; =0. When the three-phase three-wire is three-wire, the B circuit voltage does not participate in the angle calculation;
					Zxotcfg[2]: =1. The UC channel participates in the angle calculation; =0. Based on the threshold comparison results, select whether UC participates in the angle calculation.
					Zxotcfg[1]: =1. The UB channel participates in the angle calculation; =0, select whether UB participates in the angle calculation based on the threshold comparison result.
					Zxotcfg[0]: =1, the UA channel participates in the angle calculation; =0, select whether UA participates in angle calculation based on the threshold comparison results. When [2:0] is valid at the same time or both, the starting point of the angle calculation starts with UA>UB>UC.
					If it is necessary to specify whether the voltage channel participates in the angle calculation completely by the software, and does not compare it by the hardware, the following settings can be made:
					1. Zxotcfg[4]=1, select as ZXOTU;
					2.Configure ZXOTU as max value;
					3. The software sets bit2~bit0 according to needs, and freely selects whether the voltage channel participates in the angle calculation and which seat angle calculation starting point is selected.
93H	DMA_WAVECON	R/W	4	0x0	Synchronous sampling channel configuration register
94H	IN_WaveEN	R/W	2	0x0000	IN waveform buffer enable register
95H~97H	Reserved				reserved
98H	OI2_LVL	R/W	2	0x0000	Overcurrent amplitude threshold configuration register
99H	OI2_CNTT	R/W	1	0x00	Overcurrent time threshold configuration register

9AH	EMMCFG2	R/W	4	0x04	EMU configuration register 2
9BH	CFCFG1	R/W	4	0x0	CF pin configuration register 1
9CH	OV2_LVL	R/W	2	0x0000	Overvoltage amplitude threshold configuration register
9DH	OV2_CNTTH	R/W	2	0x0000	Overvoltage time threshold configuration register
9EH~ADH	Reserved				reserved
AEH	CHECKSUM 3	R	4	0xFFFC07FB	Checksum register 3
AFH	Reserved				reserved
B0H	PA_PHSM	R/W	3	0x000000	A-phase active segment phase calibration register - midsection Note: The high byte is invalid, and the read and write operation is 3 bytes. The B1H~BBH address register is the same as the B0H address
B1H	PA_PHSH	R/W	3	0x000000	A-phase active segment phase calibration register - high section
B2H	PB_PHSM	R/W	3	0x000000	B-phase active segment phase calibration register - midsection
B3H	PB_PHSH	R/W	3	0x000000	B-phase active segment phase calibration register – high section
B4H	PC_PHSM	R/W	3	0x000000	C-phase active segment phase calibration register - midsection
B5H	PC_PHSH	R/W	3	0x000000	C-phase active segment phase calibration register – high section
B6H	QA_PHSM	R/W	3	0x000000	A-phase reactive segment phase calibration register - midsection
B7H	QA_PHSH	R/W	3	0x000000	A-phase reactive segment phase calibration register – high section
B8H	QB_PHSM	R/W	3	0x000000	B-phase reactive segment phase calibration register - midsection
B9H	QB_PHSH	R/W	3	0x000000	B-phase reactive segment phase calibration register – high section

BAH	QC_PHSM	R/W	3	0x000000	C-phase reactive segment phase calibration register - midsection
BBH	QC_PHSH	R/W	3	0x000000	C-phase reactive segment phase calibration register – high section
BCH ~CAH	Reserved				reserved
CBH	LS_DCOS_IA	R/W	2	0x0	DC offset calibration during no-voltage of IA measurement
CCH	LS_DCOS_IB	R/W	2	0x0	DC offset calibration during no-voltage of IB measurement
CDH	LS_DCOS_IC	R/W	2	0x0	DC offset calibration during no-voltage of IC measurement
CEH	LS_THOA	R/W	3	0x0	No-voltage of IA measurement threshold set register
CFH	LS_THOB	R/W	3	0x0	No-voltage of IB measurement threshold set register
D0H	LS_THOC	R/W	3	0x0	No-voltage of IC measurement threshold set register
Synchronous sampling channel configuration register					
D1H	DMA_WAVECON2	R/W	4	0x3F800	Synchronous sampling channel configuration register 2
D2H	PHS_UA_WAVE	R/W	2	0x0	Synchronous sampling UA channel phase calibration register
D3H	PHS_UB_WAVE	R/W	2	0x0	Synchronous sampling UB channel phase calibration register
D4H	PHS_UC_WAVE	R/W	2	0x0	Synchronous sampling UC channel phase calibration register
D5H	PHS_IA_WAVE	R/W	2	0x0	Synchronous sampling IA channel phase calibration register
D6H	PHS_IB_WAVE	R/W	2	0x0	Synchronous sampling IB channel phase calibration register
D7H	PHS_IC_WAVE	R/W	2	0x0	Synchronous sampling IC channel phase calibration register
D8H	PHS_IN_WAVE	R/W	2	0x0	Synchronous sampling IN channel phase calibration register
D9H	GSUA_WAV	R/W	2	0x0	Simultaneous sampling UA channel gain calibration

					register
DAH	GSUB_WAVE	R/W	2	0x0	Synchronously sampling UB channel gain calibration register
DBH	GSUC_WAVE	R/W	2	0x0	Synchronously sampling UC channel gain calibration register
DCH	GSIA_WAVE	R/W	2	0x0	Synchronously sampling IA channel gain calibration register
DDH	GSIB_WAVE	R/W	2	0x0	Synchronously sampling IB channel gain calibration register
DEH	GSIC_WAVE	R/W	2	0x0	Synchronously sampling IC channel gain calibration register
DFH	GSIN_WAVE	R/W	2	0x0	Synchronously sampling IN channel gain calibration register
E0H ~E4 H	Reserved				reserved
E5H	DMA_WAVECON3	R/W	4	0x0	Waveform buffer configuration register 3
E6H	Reserved				reserved
E7H	LVDCFG	R/W	4	0x0	Voltage dip detection threshold configuration register
E8H	HW_PNum	R/W	4	0x0	Half-cycle active power calculation point configuration register
E9H	HW_QNum	R/W	4	0x0	Half-cycle reactive power calculation point configuration register
EAH	HW_MODCFG	R/W	4	0x0	Half power mode configuration register
EBH	ROS_DCATTC	R/W	4	0x0	Rogowski coil sensor integral DC attenuation factor register
ECH	ROS_Tran_K	R/W	4	0x0	Rogowski coil sensor integral conversion factor register
EDH	ROS_CFG	R/W	4	0x0	Rogowski coil sensor configuration registers
EFH	CHECKSUM4	R	4	0xF83DD8C4	Configuration the register checksum register 4
FFH	DeviceID2	R	3	0x830201	DeviceID2

3.4.Description of Configuration and Status Register

3.4.1.High-frequency Pulse Constant Register (0x00~0x01)

ADDR	5CH	00H	01H
REG	HFCONST0	HFCONST1	HFCONST2
Default	0x0	0x1000	0x1000

Bit(s)	Name	Description	R/W	Reset
15:0	HFCONST1/2	The high-frequency pulse constant register is a 2-byte unsigned number and includes two HFCONST registers, HFCONST1 and HFCONST2, HFCONST1 can be used to configure meter constants, HFCONST2 can be used for CF high-frequency pulse output when the maximum demand is calculated, or small-signal CF acceleration function when calibrating.	RW	0x1000

Each CF pin can be selected to use either HFCONST1 or HFCONST2 output pulses via the CFCFG.CFxFConst (B1 0x60) register. When comparing, compare it with the upper 16 bits of the absolute of the all-phase fast pulse counting register PTFCNT, QTFCNT, STFCNT, FPTFCNT, FQTFCNT, FFTCNT register of the upper 16 bits, if greater than or equal to the value of HFConst selected by CFCFG, then there will be a corresponding CF pulse output.

When the CF pin selects to use HFCONST2 output pulses, select whether HFCONST2 and HFCONST1 are associated by configuring the EMUCFG.HFconst2_CFG (B1 0x61). When this bit = 0, the two are not correlated; When =1, HFCONST1 and HFCONST2 are used in series, and when the pulse output configured by HFCONST1 is output, the pulse counter configured by HFCONST2 is added by 1, and when the counter value is added to the r egister of HFCONST2, the pulse configured by HFCONST2 is added by 1.

The increase in energy registers is only related to HFCONST1, not HFCONST2. For comparison, HFCONST1 is compared to the upper 16 bits of the absolute of the all-phase fast pulse count register and per-phase fast pulse counting register, and if it is greater than or equal to the value of HFConst1, the corresponding energy register is increased by 1.

The default of HFConst1 and HFConst2 are 1000H.

The calculation of HFConst refer to Chapter 4.

Bit(s)	Name	Address range	R/W	Reset
15:0	HFCONST0	The high-frequency pulse constant register 0 is a 2-byte unsigned number, =0. The per-phase high-frequency pulse constant uses the default HFCONST1 configuration; ≠0. The per-phase high-frequency pulse constant is configured independently using HFCOSNT0. When HFCONST0≠0, the upper 16 bits of the absolute of each per-phase fast pulse counting register are compared with HFCONST0, and if HFCONST0 is greater than or equal to, then the corresponding per-phase energy register is added	RW	0x0

		by 1.		

The register is used for chip configuration of the per-phase pulse constant, by WREN2 write protection, when the conjunction independently uses HFCONST1, HFCONST2 to obtain positive and reverse energy pulses, the per phase supports the independently configured high-frequency pulse constant register HFCONST0, when the per phase energy is configured in algebraic sum and accumulation mode, the positive and reverse power of the per phase can be obtained through the per phase energy register.

3.4.2.Startup Current Threshold Register (0x02~0x03)

ADDR	02H	03H
REG	IStart_PS	IStart_Q
Default	0x0250	0x0250

Bit(s)	Name	Description	R/W	Reset
15:0	IStart	In total/fundamental current RMS start-up mode IStart_PS and Start_Q are both 2-byte unsigned numbers, and when compared, they are extended to 32-bit 0x000X_XXX0 and compared with the RMS of the total current of each phase Ix or the RMS of the fundamental current FIx for the judgment of latent start-up. The calculate formulas of IStart_PS and IStart_Q are $Istart = (REGIb * (0.5 \sim 0.8)K / 2^4$ where IStart is the value of the start-up current threshold register to be set, REGIb is the register of the total or fundamental current RMS of the corrected Ib point, and K = the ratio of the starting current of a certain phase to the nominal current, if the starting current is 0.001Ib, then K=0.001. In power start-up mode 1 and 2 mode IStart_PS and IStart_Q are both 2-byte unsigned numbers, and when comparing, expand them to 24-bit 0xXXXX_00 and compare them to the absolutes of the upper 24 bits of PowerP or PowerQ (32-bit signed numbers), respectively, for starting judgment. The calculate formula of IStart_PS is: $Pstart = REGPx * (0.5 \sim 0.8) * K / 2^8$ where PStart is the IStart_PS start-up threshold register to be set, REGPx is the value of the total length per-phase active register of the corrected Ib point, and K = the ratio of a phase start-up power to nominal power, if the starting current is	RW	0x0250

0.002Ib, then K=0.002.

The calculate formula of IStart_Q is:

$$Qstart = REGQx * (0.5 \sim 0.8) * K / 2 \wedge 8$$

where QStart is the IStart_Q start-up threshold register to be set, REGQx is the total   length per-phase reactive power register of the corrected Ib point, and K = the ratio of the starting power of a certain phase to the nominal power, if the starting current is 0.002Ib, then K=0.002.

IStart_PS reset initial value and IStart_Q are the same, both are 0x250, and can be reset by the user as needed.

Provide two startup threshold registers IStart_PS and IStart_Q. The four stealth start modes are determined by the EMUCFG3.PStart_CFG and EMUCFG.NoLoadCFG configurations, and the IStart_PS and IStartQ scopes are shown in the following table:

No-load/Start-up Mode	IStart_PS	IStart_Q
Total current RMS start-up mode	Total active/apparent energy total current start-up threshold, fundamental active/apparent energy fundamental current start-up threshold	Total reactive energy total current start-up threshold, fundamental reactive energy fundamental current start-up threshold
Fundamental current RMS start-up mode	Total/fundamental, active/apparent energy fundamental current start-up threshold	Total/fundamental, reactive energy fundamental current start-up threshold
Power start-up mode 1	Total/fundamental, active/apparent/reactive energy active power start-up threshold	Total/fundamental, active/apparent/reactive energy reactive power start-up threshold
Power start-up mode 2	Total/fundamental, active/apparent energy active power start-up threshold	Total/fundamental, reactive energy reactive power start-up threshold

3.4.3.Loss of Voltage Threshold Register(0x04)

Address: 04H; word length: 2 bytes; default: 0x0400.

Bit(s)	Name	Description	R/W	Reset
15:0	LostVoltage	The loss of voltage threshold register is used to set the loss of voltage threshold of the chip, which is 2 bytes of unsigned number, and when comparing, it is compared with the 16 bits higher than the RMS of the total voltage of each phase, that is, bit27-bit12, for loss of voltage judgment. The default for LostVoltT is 0x0400. The user can reset it as needed. The calculate formula of LostVoltT: $$LostVoltT = INT((REGV_n * K) / 2 \wedge 12))$$	RW	0x400

		where REGVn is the corrected rated voltage input total RMS voltage register, K = the ratio of a phase loss voltage to the rated voltage, if the loss voltage is 50% of the rated voltage, then K = 0.5.		

3.4.4. Zero-crossing Threshold Register ZXOT (0x05)

Address: 05H; word length: 2 bytes; default: 0x0073.

Bit(s)	Name	Description	R/W	Reset
15:0	ZXOT	The zero-crossing threshold register ZXOT is a 2-byte unsigned number, and when comparing, it is compared with the RMSs of voltage and current of each phase Ux, Ix (x=A, B, C, the same below) bit27-bit12 bits for judgment. The initial Reset of the ZXOT is 0x0073, which can be reset by the user as needed. The calculate formula of ZXOT: $$ZXOT = INT((REGI_b * K) / 2 \wedge 12)$$ where REGIb is the corrected RMS current register of point Ib, K = the ratio of a phase zero crossing threshold to Ib point current, if the zero crossing threshold is 5% of the rated current, then K = 0.05.	RW	0x73

When the RMS of a channel is less than the zero-crossing threshold register, the channel does not output zero-crossing, and the phase angle of the channel is not calculated, and the phase angle of the channel outputs 0x000000.

The threshold for calculating the current angle will only use ZXOT (0x05). ZXOT (0x05) is used by default for voltage angle calculation and frequency measurement threshold, ZXOTU (0x90H) can be selected as the voltage zero-crossing and frequency measurement threshold when ZXOTCFG [4]=1 (0x92H), and ZXOT is selected as the voltage zero-crossing and frequency measurement threshold when ZXOTCFG [4]=0.

3.4.5. Phase Compensation Region Setup Register (0x06~0x09)

ADDR	06H	07H	08H	09H
REG	PRTH1L	PRTH1H	PRTH2L	PRTH2H
Default	0x0	0x0	0x0	0x0

Bit(s)	Name	Description	R/W	Reset
15:0	PRTHx	The phase compensation region setting register PRTHx is used for the segmentation angle calibration area, and there are two pairs of phase segmentation calibration current threshold PRTH registers for setting the phase calibration segment points for the small signal region and the large signal region, respectively. PRTHx is a 2-byte unsigned number, and when comparing, it is compared with the RMS of each phase	RW	0x0

		total current Ix (x=A, B, C the same below) bit27-bit12 for judgment.		

These registers PRTHx are used to set the per-phase angle difference calibration region. There are two pairs of the per-phase calibration current threshold PRTH registers with the address 0x06 - 0x09.As shown in the figure below: PRTH1L (0x06)/ PRTH1H (0x07) and PRTH2L (0x08)/ PRTH2H (0x09) can configure three per points of phase calibration regions. Region1 takes PHSx_R1 as the phase calibration parameter, Region2 takes PHSx_R2 as the phase calibration parameter, and Region3 takes PHSx_R3 as the phase calibration parameter.

In the current Ix increment direction of some phase, it takes PRTH1H as the per point of Region1 and Region2 and PRTH2H as the per point of Region2 and Region3. In the current Ix decrement direction of some phase, it takes PRTH1L as the per point of Region1 and Region2 and PRTH2L as the per point of Region2 and Region3.
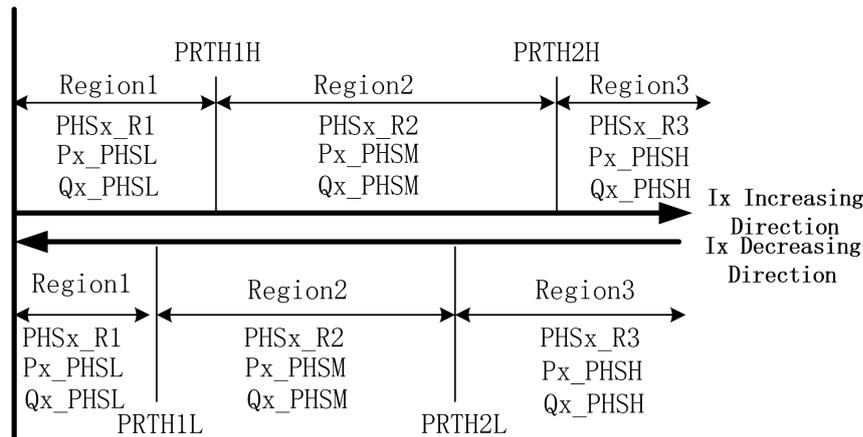
Using processes:

①To initiate fragment phase calibration, the register write order is recommended as PRTH1L(PRTH1H(PRTH2L(PRTH2H, and satisfy PRTH1L<PRTH1H<PRTH2L<PRTH2H;

②If the interval needs to be modified after fragment phase calibration is enabled, the register write value must be PRTH1L<PRTH1H<PRTH2L<PRTH2H;

Notes:

① When the PRTH1L register is 0, fragment phase calibration is not initiated. The chip current channel uses the lower 8 bits of the PHSIx register as the phase calibration value of each channel, and the power phase uses Px_PHSL and Qx_PHSL as the phase calibration value of each power;

② The PRTH1L register writes 0, clearing the PRTH1L, PRTH1H, PRTH2L, PRTH2H registers;

③ PRTH1L and PRTH1H are not 0 and PRTH1L <PRTH1H can initiate low/mid-section phase calibration;

④ When PRTH1L, PRTH1H, PRTH2L, and PRTH2H are not 0 and PRTH1L <PRTH1H<PRTH2L<PRTH2H, phase calibration can be initiated in the low, medium, and high sections;

⑤ When PRTH2L is 0, PRTH2H is not writable.

3.4.6.Current Per Region Setup Register (0x0A~0x0B)

ADDR	0AH	0BH
REG	Iregion3L	Iregion3H
Default	0x0	0x0

Bit(s)	Name	Description	R/W	Reset
15:0	Iregion3L/H	Iregion3L and Iregion3H are not associated with phase calibration registers and are only used to generate current segment flags and interrupts. The user software provides flexibility to compensate for piecemeal calibrations such as gain, phase, OFFSET, etc. using the fragmented interrupts generated by these two registers. Both registers are 2-byte unsigned numbers, which are compared to the RMS of the total current Ix(x=A,B,C)bit27-bit12 for each phase for comparison. Depending on the results of the phase current and Iregion3 threshold comparison, the corresponding flag position bit or zero of the IregionS status register. If Iregion3x interrupt is enabled, an interrupt is generated. Fault-tolerant processing: When writing to Iregion3H<Iregion3L or Iregion3L>Iregion3H, the write fails. When the Iregion3L register is 0, the function is turned off. If it is not 0, the function is started.	RW	0x0

3.4.7.Channel Phase Calibration Register (0x0C~0x12)

ADDR	0CH	0DH	0EH	0FH	10H	11H	12H
REG	PHSUA	PHSUB	PHSUC	PHSIA	PHSIB	PHSIC	PHSIN
Default	0x80	0x80	0x80	0x808080	0x808080	0x808080	0x80

Bit(s)	Name	Description	R/W	Reset
7(31):0	PHSUx	By default, it is 1 byte unsigned, and when the WREN2 register is enabled, the register is extended to 4 bytes.	RW	0x80
23(31):0	PHSIx	By default, it is 3 bytes of unsigned, and when the WREN2 register is enabled, the register is expanded to 4 bytes.	RW	0x808080

By default, the channel phase calibration register (0CH~12H) is defined as follows:

PHSUA, PHSUB, PHSUC, PHSIN is used for phase calibration of UA, UB, UC, IN. The registers are all 8-bit unsigned numbers, and the default is 0x80. At 50HZ, FOSC=8.192Mhz, 1 LSB represents *0.017578°*/LSB phase calibration.

PHSIA-PHSIC is used for segmented calibration of three phase calibration regions of three current channels in conjunction with the phase compensation region setting register PRTHx. All three registers are 24-bit unsigned numbers. In the case of PHSIA, the 3 bytes of this register are as follows:

$$\{PHSIA\_R3[23:16]，PHSIA\_R2[15:8]，PHSIA\_R1[7:0]\}$$

The lower 8 bits PHSIA_R1 [7:0] represent the phase calibration value of region 1, the middle 8 bits PHSIA_R2 [15:8] represent the phase calibration value of region 2, and the upper 8 bits PHSIA_R3 [23:16] represent the phase calibration value of region 3. The default is 0x808080.

Phase calibration rang: Under 50HZ, ±2.25° or 4.5°

Phase compensation formula:

① Through the active error calibration at 0.5L, if the power factor angle of a certain phase of 0.5L is 60°, the active error of the Ib point is err and the channel angle difference is θ, then

$$\theta = \text{Arcsin} \ \frac{-err}{\sqrt{3}}$$

If the power factor angle is 30°, the active error of the Ib point is err and the channel angle difference is θ, then

$$\theta = \text{Arcsin}(-\sqrt{3}*err)$$

For 50HZ, Both PHSUA and PHSIA register have a relationship of 0.017578°/LSB.

If you adjust the PHSUA register, there is:

$$PHSUA = 0x80+INT(\theta/0.017578°)$$

If you adjust the PHSIA registers without considering the segment calibration, you are:

$$PHSIA\_R1[7:0] = 0x80-INT(\theta/0.017578°)$$

② Using the input of one channel as the reference, the difference between the actual angle difference of Channel 1 and Reference Channel 2 being calibrated and the angle difference of the standard source or standard table is known from the phase angle register θ, If the phase register of the channel before being calibrated is PHS1, then

For 50HZ, there is the phase of the calibration channel $PHS= PHS1+INT(\theta/0.017578°)$

Note: The unit of θ is (°).

When the WREN2 register is enabled, the register expands to 4 bytes, and when the upper 8 bits of PHSUA[31:24] PHSUA[31:24] of PHSUA[31:0] (0x30) are written to the 0xA7, the meaning of all channel phase calibration registers changes, as defined as follows:

PHSUA [9:0] is UA channel phase calibration, and whenever PHSUA [31:24] writes to 0xA7, the default of PHSUA[9:0] automatically becomes 0x000 (readable as 0x000 before changing this value). Note that 0x200 is the intermediate value of the phase offset.), operation steps: first write PHSUA[31:0] to the 0xA700_0000, and then write the phase calibration value (such as PHSUA[31:0]=0xA700_02A5), note that it should be divided into two operations. In the new mode, PHSUA [31:24] should be guaranteed to remain 0xA7.

PHSUB [9:0] is UB channel phase calibration, and whenever PHSUA [31:24] writes to 0xA7, the default of PHSUB[9:0] automatically becomes 0x200 (readable as 0x000 before changing this value). Procedure: First ensure that PHSUA [31:24] has been written to the 0xA7, and then write the calibration value to PHSUB [9:0].

PHSUC[9:0] is UC channel phase calibration, and whenever PHSUA [31:24] writes to the 0xA7, the default of PHSUC [9:0] automatically becomes 0x200 (readable as 0x000 before changing this value). Procedure: First ensure that PHSUA [31:24] has been written to the 0xA7, and then write the calibration value to PHSUC [9:0].

The definition of PHSIA[31:0] was changed to {2'h0, PHSIA_R3[29:20], PHSIA_R2[19:10], PHSIA_R1[9:0]}. By default, this register is defined as described above. Once PHSUA [31:24] is written to 0xA7, its default automatically changes from 0x808080 to 0x00000000 (note that 0x20080200 is the intermediate value

of the phase offset). When PHSUA [31:24] has already written the 0xA7, write the calibration value to PHSIA [31:0].

The definition of PHSIB[31:0] was changed to {2'h0, PHSIB_R3[29:20], PHSIB_R2[19:10], PHSIB_R1[9:0]}. By default, this register is defined as described above. Once PHSUA [31:24] is written to 0xA7, its default automatically changes from 0x808080 to 0x00000000 (note that 0x20080200 is the intermediate value of the phase offset). If PHSUA [31:24] has already written to the 0xA7, the calibration value is written to PHSIB [31:0].

The definition of PHSIC[31:0] is changed to {2'h0, PHSIC_R3[29:20], PHSIC_R2[19:10], PHSIC_R1[9:0]}. By default, this register is defined as described above. Once PHSUA [31:24] is written to 0xA7, its default automatically changes from 0x808080 to 0x00000000 (note that 0x20080200 is the intermediate value of the phase offset). When PHSUA [31:24] has already written the 0xA7, write the calibration value to PHSIC [31:0].

With PHSUA [31:24] already written to 0xA7, all channel phase calibration registers were changed from 8bit to 10bit. The calibration scale was increased from 0.017578°/LSB to 0.008789°/LSB, and the calibration range was extended from ±2.25° or 4.5° to ±4.5° or 9°.

The calibration formula is the same as the default situation above, only need to modify 0.017578 to 0.008789, you can achieve a calibration range of ±4.5°. If you want to achieve a calibration range of 9°, you only need to write the register of the PHSU to 0, and then change the PHSI (from 0x000 to 0x3ff); Or write the register of PHSI to 0 and change the PHSU (from 0x000 to 0x3ff).
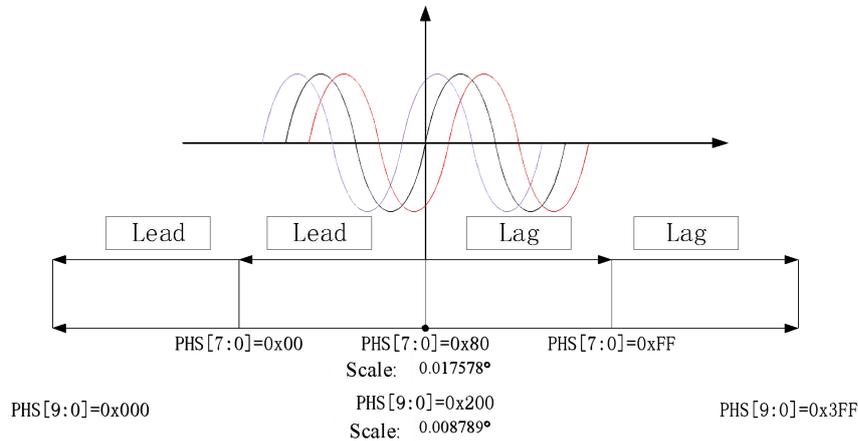
3.4.8.Channel Gain Register (0x13~0x19)

ADDR	13H	14H	15H	16H	17H	18H	19H
REG	GSUA	GSUB	GSUC	GSIA	GSIB	GSIC	GSIN
Default	0x0	0x0	0x0	0x0	0x0	0x0	0x0

Bit(s)	Name	Description	R/W	Reset
15:0	GSCH (CH: channel number)	Channel gain registers can be used for gain calibration of RMS, power. The channel gain register is a 2-byte signed number in twos complement form, with the highest bit being the sign bit, indicating the range (-1, +1).	RW	0x0

Calibration formula:

if RegGain>=2^15, then Gain=(RegGain-2^16)/2^15; otherwise Gain=RegGain/2^15; where RegGain is the channel gain register.

Taking the IB channel as an example, assume that the RMS of the B channel current IB before calibration and IB' after calibration are:IB'=IB+IB*Gain

Note that the formula valid range ensures that the signal is still within the ADC total-scale range after multiplying the channel gain.

The channel gain register is used for gain calibration in power calibration.

3.4.9.Channel DC OFFSET Calibration Register (0x1A~0x20)

ADDR	1AH	1BH	1CH	1DH	1EH	1FH
REG	DCOS_UA	DCOS_UB	DCOS_UC	DCOS_IA	DCOS_IB	DCOS_IC
Default	0x0	0x0	0x0	0x0	0x0	0x0
ADDR	20H					
REG	DCOS_IN					
Default	0x0					

Bit(s)	Name	Description	R/W	Reset
15:0	DCOS	The dc OFFSET calibration registers are 2-byte signed numbers, in twos complement form, with the highest bit being the sign bit. Effect of DCOS registers on RMSs: Under DC metering conditions, taking the IA channel as an example, the relationship between the DC DCOS_IA and the RMS of the IA channel is as follows: $IA'=IA*(1+GSIA)+DCOS\_IA*2^{12}$ Where: IA is the actual input valid value for channel A IA' is the RMS actually read out by the IA channel after calibration GSIA is the channel gain normalized value DCOS_IA is the DC offset register Instead of high-pass filtering to remove offset errors, the user	RW	0x0000

		can use the DC OFFSET auto-calibration function to obtain the DCOS register.		

Channel DC OFFSET calibration registers are used to remove offset errors in place of high-pass filtering when testing straight flows. The dc component represented by the dc OFFSET register is equivalent to superimposing the dc component directly on the sampled waveform. When DC measurement is used, the HPF needs to be turned off.

When AUTODC_EN. EMM _DC_DIS(B1 0x91[7])=1, the DCOS register has no effect on the EMU channel, only the NVM channel. By default, AUTODC_EN . EMM_DC_DIS=0.

3.4.10.RMS OFFSET Calibration Register (0x21~0x27, 0x3D~0x42)

ADDR	21H	22H	23H	24H	25H	26H	27H
REG	UA_OS	UB_OS	UC_OS	IA_OS	IB_OS	IC_OS	IN_OS
Default	0x0	0x0	0x0	0x0	0x0	0x0	0x0
ADDR	3DH	3EH	3FH	40H	41H	42H	5BH
REG	FUA_OS	FUB_OS	FUC_OS	FIA_OS	FIB_OS	FIC_OS	ISUM_OS
Default	0x0	0x0	0x0	0x0	0x0	0x0	0x0

Bit(s)	Name	Description	R/W	Reset
15:0	OFFSET	The RMS Offset calibration register is used to correct voltage/current/fundamental voltage/RMS current for small signal accuracy. The valid value of the Offset calibration register is a 2-byte signed number, in twos complement form, with the highest bit being the sign bit. The RMS Offset register only affects the RMS of the relevant channel and has an effect on apparent power and apparent energy. Calibration formula: Taking the IA channel as an example, suppose the phase A current RMS register IA before calibration and IA' after calibration, then there is: $IA' = Sqrt (Abs (IA^2 + IA\_OS*2^{14}))$	RW	0x0

Note: ISUM_OS register, which is WREN2 write protected; Other registers are WREN write-protected.

3.4.11.Power Gain Register (0x29~0x30, 0x43~0x4B)

ADDR	28H	29H	2AH	2BH	2CH	2DH	2EH

REG	GPA	GPB	GPC	GQA	GQB	GQC	GSA
Default	0x0	0x0	0x0	0x0	0x0	0x0	0x0
ADDR	2FH	30H	43H	44H	45H	46H	47H
REG	GSB	GSC	GFPA	GFPB	GFPC	GFQA	GFQB
Default	0x0	0x0	0x0	0x0	0x0	0x0	0x0
ADDR	48H	49H	4AH	4BH			
REG	GFQC	GFSA	GFSB	GFSC			
Default	0x0	0x0	0x0	0x0			

Bit(s)	Name	Description	R/W	Reset
15:0	Power_Gain	The power gain register is used for gain calibration of active/reactive/apparent active/fundamental active/fundamental reactive/fundamental apparent power. The power gain registers are 2-byte signed numbers, in twos complement form, with the highest bit being the sign bit.	RW	0x0

Calibration formula: $P1=P0(1+GP)$

$Q1=Q0(1+GQ)$

$S1=S0(1+GS)$

Among them, P1, Q1, S1 are the calibrated active, reactive, and apparent power; P0, Q0, S0 are the power before calibration; GP, GQ, and GS are normalized values for active, reactive, and apparent power gain calibration registers, respectively.

The power gain register is suitable for the traditional pulse calibration method power gain calibration, the calibration error range is -∞~50%, the calibration method is based on the A phase PF=1.0 error calibration as an example: assuming that when the A phase Ib point input, the active error reading of the standard table is err, the calculation method of the A phase active power gain calibration register GPA is as follows:

$$Gain = \frac{-Err}{1+Err}$$

If Gain>=0, then $GPA=INT[Gain*2^{15}]$; If Gain<0, then $GPA=INT[2^{16}+Gain*2^{15}]$

3.4.12.Power Phase Calibration Register (0x31~0x36, 0x4C~0x51, 0xB0~0xBB)

ADDR	31H	32H	33H	34H	35H	36H
REG	PA_PHSL	PB_PHSL	PC_PHSL	QA_PHSL	QB_PHSL	QC_PHSL
Default	0x0	0x0	0x0	0x0	0x0	0x0

ADDR	4CH	4DH	4EH	4FH	50H	51H
REG	FPA_PHS	FPB_PHS	FPC_PHS	FQA_PHS	FQB_PHS	FQC_PHS
Default	0x0	0x0	0x0	0x0	0x0	0x0
ADDR	B0H	B1H	B2H	B3H	B4H	B5H
REG	PA_PHSM	PA_PHSH	PB_PHSM	PB_PHSH	PC_PHSM	PC_PHSH
Default	0x0	0x0	0x0	0x0	0x0	0x0
ADDR	B6H	B7H	B8H	B9H	BAH	BBH
REG	QA_PHSM	QA_PHSH	QB_PHSM	QB_PHSH	QC_PHSM	QC_PHSH
Default	0x0	0x0	0x0	0x0	0x0	0x0

Bit(s)	Name	Description	R/W	Reset
15:0	Phase_Regulate1	The active power phase calibration register is used for active phase calibration on the active power channel. The reactive phase calibration register is used for reactive phase calibration on the reactive power channel. The power phase calibration register is a 2-byte signed number, with the highest bit being the sign bit.	RW	0x0

The total power phase calibration register supports power segmentation calibration in conjunction with the phase compensation area setting register PRTHx. When the PRTH1L register is 0, segmented phase calibration is not initiated; When the PRTH1L register is not equal to 0, PRTHx divides the power phase calibration region into three segments, the low region 1, the middle region 2, and the high section region 3, see Section 3.4.5.

At this time, Px_PHSL (x=A, B, C, the same below) is used for active power phase calibration in the low section of region 1, Px_PHSM for active power phase calibration in the middle section of region 2, and Px_PHSH for active power phase calibration in the high section of region 3.

Qx_PHSL (x=A, B, C, the same below) is used for reactive power phase calibration in the low section of region 1, Qx_PHSM for reactive power phase calibration in the middle section of region 2, and Qx_PHSH for reactive power phase calibration in the high section of region 3.

Calibration formula: *P2= P1+P_PHS*Q1*

Q2 = Q1-Q_PHS*P1

where P1 is the active power before compensation, P2 is the active power after compensation, Q1 is the reactive power before compensation, and Q2 is the reactive power after compensation. P_PHS, Q_PHS are normalized values of active and reactive power phase calibration registers, respectively.

Calibration method: taking phase A as an example, assuming PF=1.0, the active gain calibration of phase A has been completed; PF=0.5L, if the power factor angle is 60°, the active error of the Ib point A phase standard table is Err.

$$\lambda = \frac{-Err}{\sqrt{3}}$$

If $\lambda \geq 0$, then $PA\_PHS = \lambda *2^{15}$; If $\lambda < 0$, then $PA\_PHS = \lambda *2^{15}+2^{16}$

If $\lambda \geq 0$, then $QA\_PHS = \lambda *2^{15}$; If $\lambda < 0$, then $QA\_PHS = \lambda *2^{15}+2^{16}$

If the power factor angle is 30°, the active error of the Ib point A phase standard table is Err.

$$\lambda = -\sqrt{3} * Err$$

If $\lambda \geq 0$, then $PA\_PHS = \lambda *2^{15}$; If $\lambda < 0$, then $PA\_PHS = \lambda *2^{15}+2^{16}$

If $\lambda \geq 0$, then $QA\_PHS = \lambda *2^{15}$; If $\lambda < 0$, then $QA\_PHS = \lambda *2^{15}+2^{16}$

Note:

1. Active and reactive sectional phase calibration registers Px_PHSM, Px_PHSH, Qx_PHSM, Qx_PHSH (B1 0xB0~0xBB) and custom power register D2FP00-12 multiplexed 0xB0-0xBB address, when D2FCFG[3:0] is not equal to 4'b1001, the 0xB0-0xBB address is a mid-high active and reactive phase calibration register. When D2FCFG[3:0] equals 4'b1001, the address B1 0xA2~0xAD is used instead;

2. 0xB0~0xBB power phase calibration register is 3-byte signed number, and the remaining power phase calibration register is 2-byte signed number;

3. If the bit3 (FP_PHS_SEL) bit of EMUCFG3 (B1 0x6D) is configured as 0 in the metering unit configuration register, the fundamental power phase calibration uses a set of fundamental independent phase calibration registers (B1 0x4C~0x51), which does not have the segmentation calibration function; If the bit is configured for 1, the fundamental power phase calibration uses the same value as the total phase calibration, and if the total phase calibration is configured with the segmentation function, the fundamental also has the same function.

3.4.13. Power OFFSET Calibration Register (0x37~0x3C, 0x52~0x57)

ADDR	37H	38H	39H	3AH	3BH	3CH
REG	PA_OS	PB_OS	PC_OS	QA_OS	QB_OS	QC_OS
Default	0x0000	0x0000	0x0000	0x0	0x0	0x0
ADDR	52H	53H	54H	55H	56H	57H
REG	FPA_OS	FPB_OS	FPC_OS	FQA_OS	FQB_OS	FQC_OS
Default	0x0	0x0	0x0	0x0	0x0	0x0

Power OFFSET calibration register is divided into two categories

1. Expandable power OFFSET calibration register: PA_OS/PB_OS/PC_OS

2. Non-expandable power OFFSET calibration register.

The power OFFSET calibration register is suitable for accuracy calibration of total active/total reactive/fundamental active/fundamental reactive small signals.

The Type 1 Power OFFSET Calibration Register and the Type 2 Power OFFSET Calibration Register are both two-byte signed numbers, in twos complement form, with the highest bit being the sign bit. When WREN2 writes the expansion condition, and the EMUCFG3.P_OS_SEL (bank1 6DH bit5)=1, the PA_OS/PB_OS/PC_OS power OFFSET calibration register is the 4-byte signed number, and the checksum is calculated according to the CHECKSUM1 method before the expansion, and the checksum is calculated according to the CHECKSUM3 method after expansion; EMUCFG3. When P_OS_SEL=0, the expansion is meaningless, and the upper 16 bits are writable but the write is invalid.

Calibration formula: Taking the active power of channel A as an example, assuming that the active power register PA of channel A before the calibration is corrected, and PA' after the calibration, there is: *PA'=PA+PA_OS*.

3.4.14. Voltage Sag Threshold Register SAG (0x58)

Address: 58H; Word length: 3 bytes; Default: 000000H

Bit(s)	Name	Description	R/W	Reset
16-23	SAGCYC[7:0]	Voltage sag time threshold. See below for instructions. SAGCYC[7:0]=00H, turn off the voltage sag judgment function.	RW	0
0-15	SAGLVL[15:0]	Voltage sag peak threshold configuration. When the upper 16 bits of the peak of the absolute of a phase voltage sampling are less than SAGLVL [15:0] and the duration is SAGCYC [7:0] half-cycle wavenumber, the phase voltage sag is determined. SAGLVL[15:0]=0000H, the voltage sag judgment function is turned off.	RW	0

SAGLVL calculate formula:

$$SAGLVL = INT((\sqrt{2} * REGV_n * K) / 2 \wedge 12)$$

where REGVn is the RMS voltage register of the corrected rated voltage input, K = the ratio of a phase voltage sag voltage to the rated voltage, if the sag voltage is 10% of the rated voltage, then K=0.1.

3.4.15. Voltage Sag Threshold Register LVD (0xE7)

Address: E7H; Word length: 4 Bytes; Default: 0x0

Bit(s)	Name	Description	R/W	Reset
31:24	reserved	reserved	RO	0x0
23:16	CNTTH	**LVD time threshold configuration:** Significant bits [7:0], measured in half-cycle waves (number of half-cycle points, 80 points at 50Hz, 67 points at 60Hz). The 50Hz/60Hz select EMUCFG.FREQ_SEL (bank1 61H bit11) register bits are configured before using this register. When this register is 0, LVD detection is turned off. When this register is not 0 and PEAKTH[15:0] is not 0, LVD detection is activated. Off by default. When making LVD event judgment, this register compares the number of half-cycles with the internal sample-point counter.	RW	0x0
15:0	PEAKTH	**LVD peak threshold configuration:** The peak voltage UxPEAK_HW [15:0] of a phase voltage is less than the voltage dip detection threshold register PEAKTH [15:0], and the duration is greater than	RW	0x0000

or equal to the voltage sag detection time threshold register CNTTH [5:0] half-cycle wavenumber. Three-phase four-wire: U/UB/UC all meet the above conditions, and a three-phase four-wire LVD event occurs; Three-phase three-wire: UA/UC meets the above situation, and a three-phase three-wire LVD event occurs.

Calculation formula:

$$PEAKTH = INT((\sqrt{2} * REGV_n * K / 2 \wedge 12))$$

where REGVn is the RMS register of the nominal voltage Un after calibration of the phase voltage, and K is the voltage loss coefficient, such as K=1.2.

When this register is 0, LVD detection is turned off. When this register is not 0 and CNTTH[5:0] is not 0, LVD detection is activated. Off by default. An LVD event will cause the EMUIF2.LVD_IF (bank1 6CH) flag to be asserted, and if EMUIE2.LVD_IE=1 (bank1 6BH), LVD will be interrupted.

3.4.16.Overvoltage and Overcurrent Threshold Register

It includes the overvoltage threshold register OVLVL, OV2_LVL, OV2_CNTTH and the overcurrent threshold register OILVL, OI2_LVL, OI2_CNTTH.

3.4.16.1.Overvoltage Threshold Register OVLVL (0x59):

Address: 59H; Word length: 2 bytes; Default: 0000H

Bit(s)	Name	Description	R/W	Reset
15:0	OVLVL	This register is a 2-byte unsigned number, and when the absolute of a phase voltage sampling is 16 bits higher than OVLVL [15:0], the phase voltage is overvoltage. A phase voltage overvoltage will cause the phase OVUx(x=A,B,C) register position 1 in the PHASES register and OVIIF register 1 in the EMMIF register. If OVIIE = 1 in the EMMIE register, setting OVIIF to 1 causes an interrupt. OVIIF writes 1 to clear the zero and clear interrupt while clearing the OVUx flag. See the PHASES register and EMMIE registers and EMMIF registers for details. OVLVL[15:0]=0000H, the voltage overvoltage judgment function is turned off. OVLVL calculation formula: $$OVLVL = INT((\sqrt{2} * REGV_n * K / 2 \wedge 12))$$ where REGVn is the value of the RMS total voltage of the corrected rated voltage input, K = the ratio of overvoltage voltage and rated voltage of a certain phase, if the overvoltage voltage is 1.2 times the rated voltage, then K = 1.2.	RW	0x0

3.4.16.2.Overvoltage Threshold Register OV2_LVL (0x9C)

Address: 9CH; Word length: 2 bytes; Default: 0x0

Bit(s)	Name	Description	R/W	Reset
15:0	OV2_LVL	The half-cycle peak UxPEAK_HW of a phase voltage is greater than the overvoltage amplitude threshold register OV2_LVL [15:0], and the overvoltage duration is greater than or equal to the overvoltage time threshold register OV2_CNTTH [15:0] waves, the phase voltage overvoltage is determined. Voltage overvoltage amplitude threshold configuration register, 2-byte unsigned number, significant bit [15:0]. Calculation formula: $$OV2\_LVL = INT((\sqrt{2} * REGV_n * K / 2^{\wedge}12))$$ where REGVn is the RMS register of the nominal voltage Un after calibration of the phase voltage, and K is the overvoltage coefficient, such as K=1.2. When this register is 0, overvoltage detection is turned off. When this register is not 0 and the OV_CNTTH is not 0, the overvoltage detection function is activated. Off by default. A phase voltage overvoltage will cause the EMUIF2.OVx _IF(bank1 6CH, x=A,B,C) flag to be asserted, and if EMUIE2.OV x _IE=1 (bank1 6BH), an overvoltage interruption will occur.	RW	0x0000

3.4.16.3.Overvoltage Time Threshold Register OV2_CNTTH (0x9D)

Address: 9DH; Word length: 2 bytes; Default: 0x0

Bit(s)	Name	Description	R/W	Reset
15:0	OV2_CNTTH	Overvoltage time threshold configuration register, significant bit [15:0], in half-cycle units. The 50Hz/60Hz select EMUCFG.FREQ_SEL (bank1 61H bit11) register bits are configured before using this register. When this register is 0, overvoltage detection is turned off. When this register is not 0 and the OV_LVL is not 0, the overvoltage detection function is activated. Off by default. When an overvoltage judgment is made, this register is compared to an internal half counter.	RW	0x0

3.4.16.4.Overcurrent Threshold Register OILVL (0x5A)

Address: 5AH; Word length: 2 bytes; Default: 0000H

Bit(s)	Name	Description	R/W	Reset

Bit(s)	Name	Description	R/W	Reset
15:0	OILVL	This register is a 2-byte unsigned number, and when the absolute of a phase current sampling is 16 bits higher than OILVL [15:0], the current of the phase is judged to be overcurrent. A phase current overcurrent will cause the phase OVIx(x=A,B,C) register position 1 in the PHASES register and OVIIF register position 1 in the EMMIF register. If OVIIE = 1 in the EMMIE register, setting OVIIF to 1 causes an interrupt. OVIIF writes 1 and clear interrupts, while clearing the OVIx flag. See the PHASES register and EMMIE registers and EMMIF registers for details. If OILVL[15:0]=0000H, the overcurrent judgment function is turned off. OILVL calculate formula: $$OILVL = INT((\sqrt{2} * REGI_b * K / 2^{\wedge}12))$$ where REGIb is the corrected rated current input total RMS current register, K = the ratio of a phase overcurrent current to the rated current, if the overvoltage current is 10 times the rated current, then K = 10.	RW	0x0

3.4.16.5. Overcurrent Amplitude Threshold Register OI2_LVL (0x98)

Address: 98H; Word length: 2 bytes; Default: 0x0

Bit(s)	Name	Description	R/W	Reset
15:0	OI2_LVL	This register is used to determine the overcurrent amplitude threshold configuration register for short-circuit blackout events, 2-byte unsigned number, write protection, significant bit [15:0]. Calculate formula: $$OI2\_LVL = INT(\left(\sqrt{2} * REGI_b * \frac{K}{2^{12}}\right))$$ Among them: REGIb is the corrected nominal current Ib RMS register, and K is the short-circuit overcurrent coefficient, such as K=20. Note that in practice, if the short-circuit overcurrent amplitude threshold exceeds the ADC total-scale, the threshold can be set near the ADC total-scale. When this register is 0, short-circuit overcurrent detection is turned off. When this register is not 0 and the OI2_CNTTH is not 0, short-circuit overcurrent detection is activated. Off by default. The absolute of the peak current of a phase is greater than the short-circuit overcurrent amplitude threshold register OI2_LVL [15:0], and the duration is greater than or equal to the short-circuit overcurrent time threshold register OI2_CNTTH [5:0]*(1/8) ms, and it is determined that the phase meets the overcurrent condition of the short-circuit power outage event. A certain phase overcurrent will cause EMMIF2.	RW	0x0000

		OIx2_IF (bank1 6CH,x=A,B,C) flag set, if EMMIE2. OIx2_IE=1 (bank1 6BH), a short-circuit overcurrent interrupt for that phase is generated.		

3.4.16.6.Overcurrent Time Threshold Register OI2_CNTTH (0x99)

Address: 99H; Word length: 1 byte; Default: 0x0

Bit(s)	Name	Description	R/W	Reset
7:6	Reserved	Reserved	RO	0
5:0	OI2_CNTTH	This register is used to determine the overcurrent time threshold configuration register for short-circuit power outage events, write protected, significant bit [5:0], in 1/8ms units. When overcurrent time is judged, this register is compared to an internal OIx_CNT counter. When the absolute of the instantaneous value of a phase current is 16 bits higher than the current threshold register OI2_LVL [15:0], the internal OIx_CNT is started and counted by 1 at a rate of 8KHz. When the cumulative count OIx2_CNT count value is greater than the preset OI2_CNTTH [5:0] register, it is judged that the phase current is short-circuited and overcurrent, and the corresponding OI2x_IF interrupt flag position bit. When this register is 0, short-circuit overcurrent detection is turned off. When this register is not 0 and the OI2_LVL is not 0, short-circuit overcurrent detection is activated. Off by default.	RW	0x0

3.4.17.CF Pin Configuration Register

3.4.17.1.CF Pin Configuration Register CFCFG (0x60)

Address: 60H; Word length: 3 bytes; Default: 043210H

The CF pin configuration register CFCFG is used to configure the CF pin usage.

Bit(s)	Name	Description	R/W	Reset
23:22	Reserved	Reserved	RO	0
21	CFFSCfg	When CF1:5 Cfg [2:0] is configured as fundamental convergence, it is valid at pulse output. =0, the fundamental all-phase apparent pulse selected by CF is regarded as RMS type. =1, the fundamental all-phase apparent pulse selected by CF is PQS type. The default is 0.	RW	0
20	CFSCfg	When CF1:5 Cfg [2:0] is configured as conjunction, it is valid at pulse output. =0, the all-phase apparent pulse selected by CF is RMS	RW	0

		type. =1, the all-phase apparent pulse selected by CF is PQS type. The default is 0.		
19	CF5FConst	CF5 high frequency pulse selection. =0, with HFCONST1 as the high-frequency pulse constant output pulse. =1, with HFCONST2 as the high-frequency pulse constant output pulse. The default is 0. This bit is valid when CF5Cfg [2:0] is configured as 3'b000-3'b101, otherwise it is invalid. Same below.	RW	0
18:16	CF5Cfg [2:0]	CF5 output pulse control bit。 {{TABLE1}}	RW	3'b100
15	CF4FConst	CF4 high frequency pulse selection. =0, with HFCONST1 as the high-frequency pulse constant output pulse. =1, with HFCONST2 as the high-frequency pulse constant output pulse. The default is 0.	RW	0
14:12	CF4Cfg [2:0]	CF4 output pulse control bit {{TABLE2}}	RW	3'b011

TABLE1:

Configuration	Description
3'b000	Output total active pulse.
3'b001	Output total reactive pulse
3'b010	Output total all-phase apparent pulse. The CFSCfg register bit selects whether the convergence pulse is RMS or PQS, the same below.
3'b011	Output fundamental active pulse
3'b100 (default)	Output fundamental reactive pulse
3'b101	The output is fundamental all-phase apparent pulse. The CFFSCfg register bit selects whether the convergence pulse is RMS or PQS, the same below.
3'b110	Reserved
3'b111	Disable the CF5 pin from output pulses.

TABLE2:

Configuration	Description
3'b000	Output total active pulse.

		3'b001	Output total reactive pulse		
		3'b010	Output total all-phase apparent pulse. The CFSCfg register bit selects whether the convergence pulse is RMS or PQS, the same below.		
		3'b011 (default)	Output fundamental active pulse		
		3'b100	Output fundamental reactive pulse		
		3'b101	The output is fundamental all-phase apparent pulse. The CFFSCfg register bit selects whether the convergence pulse is RMS or PQS, the same below.		
		3'b110	Reserved		
		3'b111	Disable the CF4 pin from output pulses.		
11	CF3FConst	CF3 high frequency pulse selection. =0, with HFCONST1 as the high-frequency pulse constant output pulse. =1, with HFCONST2 as the high-frequency pulse constant output pulse. The default is 0.		RW	0
10:8	CF3Cfg[2:0]	CF3 output pulse control bit		RW	3'b010

CF3 output pulse control bit

Configuration	Description
3'b000	Output total active pulse.
3'b001	Output total reactive pulse
3'b010 (default)	Output total apparent pulse
3'b011	Output fundamental active pulse.
3'b100	Output fundamental reactive pulse
3'b101	Output fundamental apparent pulse
3'b110	Reserved
3'b111	Disables the output pulse of the CF3 pin.

7	CF2FConst	CF2 High frequency pulse selection. =0, with HFCONST1 as the high-frequency pulse constant output		RW	0

		pulse. =1, with HFCONST2 as the high-frequency pulse constant output pulse. The default is 0.		
6:4	CF2Cfg[2:0]	CF2 output pulse control bit. 	Configuration	Description
---	---
3'b000	Output total active pulse.
3'b001 (default)	Output total reactive pulse
3'b010	Output total apparent pulse
3'b011	Output fundamental active pulse.
3'b100	Output fundamental reactive pulse
3'b101	Output fundamental apparent pulse
3'b110	Reserved
3'b111	Disables the output pulse of the CF2 pin.		RW	3'b001
3	CF1FConst	CF1 high frequency pulse selection. =0, with HFCONST1 as the high-frequency pulse constant output pulse. =1, with HFCONST2 as the high-frequency pulse constant output pulse. The default is 0.	RW	0
2:0	CF1Cfg[2:0]	CF1 output pulse control bit. 	Configuration	Description
---	---
3'b000 (default)	Output total active pulse.
3'b001	Output total reactive pulse
3'b010	Output total apparent pulse
3'b011	Output fundamental active pulse.
3'b100	Output fundamental reactive pulse
3'b101	Output fundamental apparent pulse
3'b110	Reserved
3'b111	Disables the output pulse of the CF1 pin.		RW	0

3.4.17.2.CF Pin Configuration Register 1 CFCFG1 (0x9B)

Address: 9BH; Word length: 4 bytes; Default: 0x00

This register is WREN2 write protected and participates in the CHECKSUM3 checksum, which defaults to 0 and does not affect the checksum default. The register is configured with the data source of CF6, CF7 and CF8, which can output the metering pulse corresponding to the phase division of A, B and C respectively, and output it from the CF1~CF5 pin by configuring the D2FCFG register.

Bit(s)	Name	Description	R/W	Reset
31:12	Reserved	Reserved.	RO	0
11:8	CF8CFG[3:0]	CF8 output pulse control bit. 	Configuration	Description
---	---
3'b000	CF8 defaults to D2F pulses
3'b001	Output C-phase total active pulse.
3'b010	Output C-phase total reactive pulse.
3'b011	Output C-phase apparent active pulse.
3'b100	Output C-phase fundamental active pulse.
3'b101	Output C-phase fundamental reactive pulse.
3'b110	Output C-phase fundamental apparent pulse.
Others	No pulse output		RW	0
7:4	CF7CFG[3:0]	CF7 output pulse control bit. 	Configuration	Description
---	---
3'b000	CF7 defaults to D2F pulses
3'b001	Output B-phase total active pulse.
3'b010	Output B-phase total reactive pulse.
3'b011	Output B-phase apparent active pulse.
3'b100	Output B-phase fundamental active pulse.
3'b101	Output B-phase fundamental reactive pulse.		RW	0

		3'b110	Output B-phase fundamental apparent pulse.		
		Others	No pulse output		
3:0	CF6CFG[3:0]	CF7 output pulse control bit. 	Configuration	Description
---	---
3'b000	CF6 defaults to D2F pulses
3'b001	Output A-phase total active pulse.
3'b010	Output A-phase total reactive pulse.
3'b011	Output A-phase apparent active pulse.
3'b100	Output A-phase fundamental active pulse.
3'b101	Output A-phase fundamental reactive pulse.
3'b110	Output A-phase fundamental apparent pulse.
Others	No pulse output		RW	0

3.4.18. Measurement Unit Configuration Register

3.4.18.1. EMMCFG Register (0x61)

Address: 61H; Word length: 3 bytes; Default: 0x400000

The measurement unit configuration register EMUCFG is used to configure the metering module.

Bit(s)	Name	Description	R/W	Reset
23:22	Reserved	The original CTT frequency configuration function is removed, but the register read and write properties and Resets are retained.	RW	01
21	EQADDMOD0	This bit, together with the EMUCFG3.EQADDMOD1 bit, determines the conjunction non-functional accumulation method selection. {EQADDMOD1,EQADDMOD0} =2'b00, algebra accumulation mode; =2'b01, absolute accumulation mode; =2'b10, positive accumulation mode; =2'b11, negative accumulation mode. Read MODSEL(Bank1 86H)=0, i.e. when selecting a three-phase four-wire system, this bit is configurable and	RW	0

		the default is 0. Read MODSEL(Bank1 86H)=1, that is, when the three-phase three-wire system is selected, this bit is written invalidly, and it is always 0.		
20	EPADDMOD 0	This bit, together with the EPADDMOD1 bit, determines the conjunction with functional quantity accumulation mode selection. {EMUCFG3.EPADDMOD1,EPADDMOD0} =2'b00, algebra accumulation mode; =2'b01, absolute accumulation mode; =2'b10, positive accumulation mode; =2'b11, negative accumulation mode. Read MODSEL(Bank1 86H)=0, i.e. when selecting a three-phase four-wire system, this bit is configurable and the default is 0. Read MODSEL(Bank1 86H)=1, that is, when the three-phase three-wire system is selected, this bit is written invalidly, and it is always 0.	RW	0
19	ERegCAR	Energy register type selection. =0, zero-type after reading. =1, additive. The default is 0.	RW	0
18	ISUMMOD	Current vector and calculation method selection. =0, the null line current does not participate in the calculation; =1, the null current participates in the calculation. Read MODSEL(Bank1 86H)=0, i.e. when selecting a three-phase four-wire system, this bit is configurable and the default is 0. Read MODSEL(Bank1 86H)=1, that is, when the three-phase three-wire system is selected, this bit is written invalidly, and it is always 0.	RW	0
17	Reserved	Reserved.	RW	0
16	NoLoadCFG	Start-up mode selection. =0, total start-up is judged by comparing the RMS of total current with the start-up threshold. =1, total start-up is judged by comparing the RMS fundamental current with the start-up threshold. The default is 0.	RW	0
15	SAGINT_CF G	The default is 0. =0 Three-phase four-wire: if any phase of the polyphase voltage temporarily drops, it will be interrupted; Three-phase three-wire: N/A. =1 Three-phase four-wire: all polyphase voltages are sagged	RW	0

		before interruption; Three-phase three-wire: all the voltages of A/C channels are sagged before they are interrupted, and B channels do not participate.		
14:12	Reserverd	Reserved.	RW	0
11	FREQ_SEL	=0: SAG, short circuit, overvoltage, overcurrent, undervoltage, LVD, 50Hz period; =1: SAG, short circuit, overvoltage, overcurrent, undervoltage, LVD, 60Hz period.	RW	0
10:8	Reserved	Reserved.	RW	0
7	HFCONST2_CFG	The default is 0; =0: HFCONST1 and HFCONST2 are used independently; =1: HFCONST1 and HFCONST2 are used in series, when the pulse output configured by HFCONST1, the pulse counter configured by HFCONST2 is added by 1, and when the counter accumulates to the register of HFCONST2, the pulse configured by HFCONST2 is added by 1.	RW	0
6:0	HPFOFF[6:0]	The sampling channel {IN, IC, IB, IA, UC, UB, UA} high-pass filter enable select bits. =0, select Qualcomm Enable; =1, select Qualcomm ban. Default state=7'b00000000, select Qualcomm Enable.	RW	0

3.4.18.2.EMUCFG2 Register (0x9A)

Address: 9AH; Word length: 4 bytes; Default: 0x4.

EMUCFG2 is used to configure the metering module for per-phase total /fundamental active/reactive power mode selection, half-cycle RMS and half power calculation.

Bit(s)	Name	Description	R/W	Reset
31	FQ_HW_SEL	=0, the instantaneous fundamental reactive power integration is used for fundamental reactive energy calculation; =1, the fundamental reactive energy calculation adopts the half-cycle update of the fundamental reactive power integration; At the same time, SPL_FQx output half-cycle updated total active power.	RW	0
30	FP_HW_SEL	=0, the instantaneous fundamental active power integration is used for fundamental active energy calculation; =1, the fundamental active energy calculation adopts the half-cycle update of the fundamental active power integration; At the same time, SPL_FPx output half-cycle	RW	0

		updated total active power.		
29	Q_HW_SEL	=0, the instantaneous total reactive power integration is used for the calculation of total reactive energy; =1, the total reactive energy calculation adopts the total reactive power integration updated half-cycle; At the same time, SPL_Qx output half-cycle updated total active power.	RW	0
28	PQST_SEL	=0 (default), the data accumulation source of PQS all-phase apparent energy is instantaneous all-phase PQS apparent power (including instantaneous 8KHz update power and half-cycle update power); =1, the data accumulation source of PQS all-phase apparent energy is the average all-phase PQS apparent power;	RW	0
27:26	FQCCnt_Mode	=2'b00 C-phase fundamental reactive algebra accumulation mode; =2'b01 C-phase fundamental reactive absolute accumulation mode; =2'b10 C-phase fundamental reactive positive accumulation mode; =2'b11 C-phase fundamental reactive negative accumulation mode;	RW	0
25:24	QCCnt_Mode	=2'b00 C-phase reactive algebra accumulation mode; =2'b01 C-phase reactive algebra accumulation mode; =2'b10 C-phase reactive positive accumulation mode; =2'b11 C-phase reactive negative accumulation mode;	RW	0
23:22	FQBCnt_Mode	=2'b00 B-phase fundamental active algebra accumulation mode; =2'b01 B-phase fundamental reactive absolute accumulation mode; =2'b10 B-phase fundamental reactive positive accumulation mode; =2'b11 B-phase fundamental reactive negative accumulation mode;	RW	0
21:20	QBCnt_Mode	=2'b00 B-phase reactive algebra accumulation mode; =2'b01 B-phase reactive algebra accumulation mode; =2'b10 B-phase reactive positive accumulation mode;	RW	0

		=2'b11 B-phase reactive negative accumulation mode;		
19:18	FQACnt_Mode	=2'b00 A-phase fundamental reactive algebra accumulation mode; =2'b01 A-phase fundamental reactive absolute accumulation mode; =2'b10 A-phase fundamental reactive positive accumulation mode; =2'b11 A-phase fundamental reactive negative accumulation mode;	RW	0
17:16	QACnt_Mode	=2'b00 A-phase reactive algebra accumulation mode; =2'b01 A-phase reactive algebra accumulation mode; =2'b10 A-phase reactive positive accumulation mode; =2'b11 A-phase reactive negative accumulation mode;	RW	0
15:14	FPCCnt_Mode	=2'b00 C-phase fundamental active algebra accumulation mode; =2'b01 C-phase fundamental active absolute accumulation mode; =2'b10 C-phase fundamental active positive accumulation mode; =2'b11 C-phase fundamental active negative accumulation mode;	RW	0
13:12	PCCnt_Mode	=2'b00 C-phase active algebra accumulation mode; =2'b01 C-phase active algebra accumulation mode; =2'b10 C-phase active positive accumulation mode; =2'b11 C-phase active negative accumulation mode;	RW	0
11:10	FPBCnt_Mode	=2'b00 B-phase fundamental active algebra accumulation mode; =2'b01 B-phase fundamental active absolute accumulation mode; =2'b10 B-phase fundamental active positive accumulation mode; =2'b11 B-phase fundamental active negative accumulation	RW	0

Bits	Name	Description	Access	Reset
		mode;		
9:8	PBCnt_Mode	=2'b00 B-phase active algebra accumulation mode; =2'b01 B-phase active algebra accumulation mode; =2'b10 B-phase active positive accumulation mode; =2'b11 B-phase active negative accumulation mode;	RW	0
7:6	FPACnt_Mode	=2'b00 A-phase fundamental active algebra accumulation mode; =2'b01 A-phase fundamental active absolute accumulation mode; =2'b10 A-phase fundamental active positive accumulation mode; =2'b11 A-phase fundamental active negative accumulation mode;	RW	0
5:4	PACnt_Mode	=2'b00 A-phase active algebra accumulation mode; =2'b01 A-phase active algebra accumulation mode; =2'b10 A-phase active positive accumulation mode; =2'b11 A-phase active negative accumulation mode;	RW	0
3	P_HW_SEL	=0, the instantaneous active power integration is used for active energy calculation. =1, the active energy calculation adopts the half-cycle active power integration method, and the SPL_Px register is multiplexed into a half-cycle active power register.	RW	0
2	RMS_HW_CFG	=1, the half-cycle RMS is calculated by selecting the total voltage zero crossing point. =0 the half-cycle RMS is calculated by selecting the fundamental voltage zero crossing point.	RW	1
1	P_HW_CFG	=1, the half-cycle active power is calculated by selecting the total voltage zero crossing point. =0 the half-cycle active power is calculated by selecting the fundamental voltage zero crossing point.	RW	0
0	RMS_HW_SQRT	=0: The 32-bit half-cycle RMS register represents the result after the original waveform is squared, 32 bits are valid, and a software root-open number is required to obtain the half-cycle RMS. =1: The 32-bit half-cycle RMS register	RW	0

		represents the result of the root-opening number, the lower 24 bits are valid and the upper 8 bits are fixed at 0.		

3.4.18.3.EMUCFG3 Register (0x6D)

Address: 6DH; Word length: 4 bytes; Default:0x0.

EMUCFG3 is used to configure the metering module.

Bit(s)	Name	Description	R/W	Reset
31	Reserved	Reserved.	RO	0
27	Sx_SEL	Per-phase apparent power selection of configuration bits. =0, per-phase in electrical energy, fast pulse counting selection as per-phase apparent RMS ; =1, the phase is divided in the electric energy, and the fast pulse counting is selected as PQS in the phase; Affected registers: ESx, FESx, SxFCnt, FSxFCnt	RW	0
26	Reserved	Reserved.	RW	0
25	FQT_Sign_SEL	=0 (default), three-phase four-wire mode, the all-phase fundamental reactive power accumulation symbol is selected as the average all-phase fundamental reactive power symbol; =1, three-phase four-wire mode, the all-phase fundamental reactive power accumulation symbol is selected as the instantaneous all-phase phase fundamental reactive power symbol;	RW	0
24	QT_Sign_SEL	=0 (default), three-phase four-wire mode, all-phase total reactive power accumulation symbol is selected as average confluent total reactive power symbol; =1, three-phase four-wire mode, the all-phase total reactive power accumulation symbol is selected as the instantaneous combined total reactive power symbol;	RW	0
23	FPT_Sign_SEL	=0 (default), three-phase four-wire mode, the all-phase fundamental active accumulation symbol is selected as the average all-phase fundamental active power symbol; =1, three-phase four-wire mode, the all-phase fundamental active accumulation symbol is selected as the instantaneous all-phase fundamental active power symbol;	RW	0
22	PT_Sign_SEL	=0, three-phase four-wire mode, the all-phase total active accumulation symbol is selected as the average confluent total active power symbol; =1. In the three-phase four-wire mode, the all-phase total active accumulation symbol is selected as the instantaneous all-phase total active power symbol;	RW	0

21	Freq_Cycle	=0, UFreq voltage line frequency register (Bank 57H) update period is 32 cycles; =1, the UFreq voltage line frequency register (Bank0 57H) update period is 1 cycle;	RW	0
20	PQS_FSTRUN	=0, PQS all-phase fundamental vision is turned on in energy measurement; =1, PQS all-phase fundamental apparent energy metering off;	RW	0
19	PQS_STRUN	=0, PQS all-phase total apparent energy measurement is enabled; =1, PQS all-phase total apparent energy measurement is off;	RW	0
18	EQADDMOD1	This bit and the EMMCFG.EQADDMOD0 bit determine the conjunction non-functional accumulation method selection, which is described in EMMCFG.EQADDMOD0. Read MODSEL(Bank1 86H)=1, that is, when the three-phase three-wire system is selected, this bit is written invalidly, and it is always 0. Read MODSEL(Bank1 86H)=0, i.e. when selecting a three-phase four-wire system, this bit is configurable and the default is 0.	RW	0
17	EPADDMOD1	This bit and the EPADDMOD0 bit together determine the choice of the functional accumulation method of the conjunction, which is described in EPADDMOD0. Read MODSEL(Bank1 86H)=1, that is, when the three-phase three-wire system is selected, this bit is written invalidly, and it is always 0. Read MODSEL(Bank1 86H)=0, i.e. when selecting a three-phase four-wire system, this bit is configurable and the default is 0.	RW	0
16	FLK_SEL	=0,FLK_Ux_5 Instantaneous sampling of the voltage channel stored in the FIFO; =1,FLK_Ux_5 Instantaneous flicker values are stored in the FIFO.	RW	0
15	FLKCAL_EN	=0, the flicker module is not calculated; =1, the flicker module starts the calculation. When changing from 0 to 1, the flicker module computing unit is reset	RW	0
14:10	Reserved	Reserved.	RW	0
9:8	PStart_CFG[1:0]	=0x: The RMS current start-up mode is adopted, and the measurement of the active/reactive/apparent power of the phase is initiated when the per-phase current exceeds the	RW	0

		threshold.		
		=10: Using power start mode 1, the phase metering is started if the per-phase active power or reactive power exceeds the threshold, and the phase metering is turned off if the per-phase active power and reactive power are lower than the threshold. The power threshold register is multiplexed with the start-up current register.		
		=11: Using the power start mode 2, the per-phase active power exceeds the threshold to start the phase active power measurement, the per-phase reactive power exceeds the threshold to start the phase reactive power, as long as one exceeds the threshold then start the phase of the apparent, that is: the active and reactive threshold are separated.		
7:6	WAVUD_CFG	=00: Waveform sampling interrupts 8Khz rate refresh; =01: Waveform sampling interrupts 4Khz rate refresh; =10: Waveform sampling interrupts 2Khz rate refresh; =11: Waveform sampling interrupts 1Khz rate refresh;	RW	0
5	P_OS_SEL	=0PA_OS/PB_OS/PC_OS is 16-bit signed number; =1: And WREN2 expands, PA_OS/PB_OS/PC_OS is a 32-bit signed number;	RW	0
4	ANGLE_FREQ	=0: The update time of the angle register is 32 cycles, about 640ms. =1: The update time of the angle register is 1 cycle, about 20ms.	RW	0
3	FP_PHS_SEL	=0: Fundamental power phase calibration uses a set of fundamental independent phase calibration registers (4CH~51H), which does not have a segmented calibration function; =1: Fundamental power phase calibration uses the same value for total phase calibration, and if total phase calibration is configured with segmentation, the fundamental also has the same function.	RW	0
2	FIN_SEL_IN	=0IN register output is a null line total RMS; =1: IN register output is a null line fundamental RMS;	RW	0
1	FIN_SEL_USUM	=0: USUM register output is the voltage vector sum; =1: USUM register output is null line fundamental RMS	RW	0

0	HWCAL_EN	Simultaneous sampling channel half-cycle RMS 2 calculation enable; =0, half-cycle RMS 2 module does not calculate; =1, half-cycle RMS 2 module start to calculate; When changing from 0 to 1, the half-cycle RMS 2 module calculation unit will be reset.	RW	0

3.4.18.4. EMUCFG4 Register (0x6E)

Address: 6EH; Word length: 4 Bytes; Default: 0x0.

This register is write-protected by WREN2, and [15:0] of this register determines the convergence fast pulse integration method (affecting the all-phase fast pulse counting register, the all-phase energy register). Among them, the algebraic sum and integral mode refer to the positive pulse counting in the positive (+) direction and the negative pulse according to the negative (-) count when the all-phase fast pulse is counted; The absolute integration method means that when the all-phase fast pulse is counted, the positive pulse is counted in the positive direction, and the negative direction is also counted according to the positive +; The positive integration method means that the all-phase fast pulse counting only counts the positive pulse, and the negative pulse is discarded; The negative integration method means that the all-phase fast pulse counting only counts the negative pulse, and counts the negative pulse according to the positive direction, and the positive pulse is discarded.

Note: The combined fast pulse integration method of this register configuration is different from the combined active/reactive power accumulation method jointly determined by EMUCFG3 [17:18] and EMUCFG [20:21].

Bit(s)	Name	Description	R/W	Reset
31:22	Reserved	Reserved.	RO	0
21:20	USUM_CSign	=00, the factor of $u_C(t)$ in formula U_{SUM} is 1; =01, the factor of $u_C(t)$ in formula U_{SUM} is -1; =others, the factor of $u_C(t)$ in formula U_{SUM} is 0;	RW	0
19:18	USUM_BSign	=00, the factor of $u_B(t)$ in formula U_{SUM} is 1; =01, the factor of $u_B(t)$ in formula U_{SUM} is -1; =others, the factor of $u_B(t)$ in formula U_{SUM} is 0;	RW	0
17:16	USUM_ASign	=00 (default), the factor of $u_A(t)$ in formula U_{SUM} is 1; =01, the factor of $u_A(t)$ in formula U_{SUM} is -1; =others, the factor of $u_A(t)$ in formula U_{SUM} is 0;	RW	0

15:14	FQ_ADDMOD_HF2	=00, the all-phase fundamental reactive fast pulse independently configured by HFCONST2 is algebraic sum and integral mode; =01, the convergence fundamental reactive fast pulse independently configured by HFCONST2 is the absolute integration mode; =10, the combined fundamental reactive fast pulse independently configured by HFCONST2 is the positive integration mode; =11, The combined fundamental reactive fast pulse independently configured by HFCONST2 is a negative integration mode;	RW	0
13:12	FP_ADDMOD_HF2	=00, the all-phase fundamental active fast pulse independently configured by HFCONST2 is algebraic sum and integral mode; =01, the all-phase fundamental active fast pulse independently configured by HFCONST2 is absolute integration mode; =10, the all-phase fundamental active fast pulse is independently configured by HFCONST2 as the positive integration mode; =11, the all-phase fundamental active fast pulse independently configured by HFCONST2 is a negative integration mode;	RW	0
11:10	Q_ADDMOD_HF2	=00, the all-phase total reactive fast pulse independently configured by HFCONST2 is algebraic sum and integral mode; =01, the all-phase total reactive fast pulse independently configured by HFCONST2 is absolute integration mode; =10, the all-phase total reactive fast pulse is independently configured by HFCONST2 as the positive integration mode; =11, the all-phase total reactive fast pulse independently configured by HFCONST2 is a negative integration mode;	RW	0
9:8	P_ADDMOD_HF2	=00, the all-phase total active fast pulse independently configured by HFCONST2 is algebraic sum and integral mode; =01, the all-phase total active fast pulse independently configured by HFCONST2 is absolute integration mode; =10, the all-phase total active fast pulse is independently configured by HFCONST2 as the positive integration mode; =11, the all-phase total active fast pulse independently configured by HFCONST2 is a negative integration	RW	0

		mode;		
7:6	FQ_ADDMOD_HF1	=00, the all-phase fundamental reactive fast pulse independently configured by HFCONST1 is algebraic sum and integral mode; =01, the all-phase fundamental reactive fast pulse independently configured by HFCONST1 is absolute integration mode; =10, the all-phase fundamental reactive fast pulse is independently configured by HFCONST1 as the positive integration mode; =11, the all-phase fundamental reactive fast pulse independently configured by HFCONST1 is a negative integration mode;	RW	0
5:4	FP_ADDMOD_HF1	=00, the all-phase fundamental active fast pulse independently configured by HFCONST1 is algebraic sum and integral mode; =01, the all-phase fundamental active fast pulse independently configured by HFCONST1 is absolute integration mode; =10, the all-phase fundamental active fast pulse is independently configured by HFCONST1 as the positive integration mode; =11, the all-phase fundamental active fast pulse independently configured by HFCONST1 is a negative integration mode;	RW	0
3:2	Q_ADDMOD_HF1	=00, the all-phase total reactive fast pulse independently configured by HFCONST1 is algebraic sum and integral mode; =01, the all-phase total reactive fast pulse independently configured by HFCONST1 is absolute integration mode; =10, the all-phase total reactive fast pulse is independently configured by HFCONST1 as the positive integration mode; =11, the all-phase total reactive fast pulse independently configured by HFCONST1 is a negative integration mode;	RW	0
1:0	P_ADDMOD_HF1	=00, the all-phase total active fast pulse independently configured by HFCONST1 is algebraic sum and integral mode; =01, the all-phase total active fast pulse independently configured by HFCONST1 is absolute integration mode; =10, the all-phase total active fast pulse is independently configured by HFCONST1 as the positive integration mode;	RW	0

| | | =11, the all-phase total active fast pulse independently configured by HFCONST1 is a negative integration mode; | | |

3.4.18.5. Measurement Special Function Configuration Register SPECFG (0x6F)

Address: 6FH; Word length: 4 bytes; Default: 0x0.

Controlled by WREN2 write enable, it participates in CHECKSUM3 verification.

Bit(s)	Name	Description	R/W	Reset
31:24	PSW	Write the password bit, the password is 0xEA; =0xEA, bit0~bit2 are writable; =others, bit0~bit2 are not writable;	RW	0
23:3	Reserved	Reserved.	RO	0
2	EMU_mod_adapt	=0, does not enable three-phase three-wire and three-phase four-wire adaptation; =1 to enable three-phase three-wire and three-phase four-wire adaptation.	RW	0
1	B_force_cal	=0, phase B is not forced to participate in measurement; =1, phase B is forced to participate in metering, focusing on participating in energy integration, independent of PRUN/QRUN, no-load/start-up and MODSEL. All related to the start of phase B is forced to start.	RW	0
0	UB_Sel	=0, select the default 3P3, 3P4 energy algorithm; =1, select the $U_b = -U_a - U_c$ algorithm;	RW	0

3.4.19. Measurement Control Register EMUCON (0x62)

Address: 62H; Word length: 3 bytes; Default: 0x000000

The measurement control register EMUCON is used to control the active/reactive/RMS apparent / fundamental active / fundamental reactive / fundamental apparent energy measurement enabled off for each phase (A/B/C).

Bit(s)	Name	Description	R/W	Reset
23	Reserved	Reserved.	RO	0x0
22:20	FSRUN[2:0]	C/B/A phase fundamental apparent active energy measurement enable bit. FSRUNx=1, enable the phase RMS fundamental energy apparent metering, and the phase RMS fundamental apparent participation	RW	0x0

		in the RMS all-phase fundamental apparent energy calculation. FSRUNx=0, turn off the phase RMS fundamental energy apparent metering, and the phase RMS fundamental apparent does not participate in the RMS all-phase fundamental apparent energy calculation. The default state is 3'b000.		
19	Reserved	Reserved.	RO	0x0
18:16	FQRUN[2:0]	C/B/A phase fundamental reactive energy measurement enable bit。 FQRUNx=1, enable the phase fundamental apparent reactive energy metering, and the phase fundamental reactive energy participation in the all-phase fundamental reactive energy calculation. FQRUNx=0, turn off the phase fundamental reactive energy apparent metering, and the phase fundamental reactive energy does not participate in the all-phase fundamental reactive energy calculation. The default state is 3'b000.	RW	0x0
15	Reserved	Reserved.	RO	0x0
14:12	FPRUN[2:0]	C/B/A phase fundamental active energy measurement enable bit. FPRUNx=1, enable the phase fundamental active energy measurement, and the phase fundamental active energy participates in the all-phase fundamental active energy calculation. FPRUNx=0, turn off the phase fundamental active energy measurement, and the phase fundamental active energy does not participate in the all-phase fundamental active energy calculation. The default state is 3'b000.	RW	0x0
11	Reserved	Reserved.	RO	0x0
10:8	SRUN[2:0]	C/B/A phase apparent energy measurement enable bit. SRUNx=1, enable the phase RMS apparent energy measurement, and the phase RMS apparent energy participates in the RMS all-phase apparent active energy calculation. SRUNx=0, turn off the phase RMS apparent energy measurement, and the phase RMS apparent energy does not participate in the RMS all-phase apparent active energy calculation. The default state is 3'b000.	RW	0x0
7	Reserved	Reserved.	RO	0x0
6:4	QRUN[2:0]	C/B/A phase reactive energy measurement enable bit. QRUNx=1, enable the measurement of reactive energy of the phase, and the reactive energy of the phase participates in the calculation of the all-phase reactive energy. QRUNx=0, turn off the measurement of reactive energy of the phase, and the reactive energy of the phase does not participate in the calculation of the all-phase reactive energy. The default state	RW	0x0

		is 3'b000.		
3	Reserved	Reserved.	RO	0x0
2:0	PRUN[2:0]	C/B/A phase active energy measurement enable bit. PRUN0 controls phase A, PRUN1 controls phase B, and PRUN2 controls phase C. This bit does not affect power and RMS calculations, only per-phase and confluent-phase active energy measurement. Same as above. PRUNx=1, enable the measurement of the active energy of the phase, and the active energy of the phase participates in the calculation of the all-phase active energy. PRUNx=0, turn off the measurement of the active energy of the phase, and the active energy of the phase does not participate in the calculation of the all-phase active energy. The default state is 3'b000.	RW	0x0

3.4.20.D2F Register

3.4.20.1.D2FCFG Register (0x95)

Address: 95H; Word length: 2 bytes; Default: 0x0H

The custom energy pulse configuration registers are defined below:

Bit(s)	Name	Description	R/W	Reset
15	Reserved	Reserved.	RO	0
14	HFCONST3_CFG	=0: HFCONST3 must be set to an integer multiple of 4, under the same conditions, the relationship with HFCONST1 is HFCONST3=4*HFCONST1; =1: HFCONST3 does not have to be set to an integer multiple of 4, under the same conditions, the relationship with HFCONST1 is HFCONST3=HFCONST1;	RW	0
13:12	CF5_UDef	=00, CF5 output refers to the CFCFG (bank1 60H) register definition; =01, CF5 output custom pulse CF6; =10, CF5 output custom pulse CF7; =11, CF5 output custom pulse CF8;	RW	0
11:10	CF4_UDef	=00, CF4 output refers to the CFCFG (bank1 60H) register definition; =01, CF4 output custom pulse CF6; =10, CF4 output custom pulse CF7; =11, CF4 output custom pulse CF8;	RW	0

Bit(s)	Name	Description	R/W	Reset
9:8	CF3_UDef	=00, CF3 output refers to CFCFG (bank1 60H) register definition; =01, CF3 output custom pulse CF6; =10, CF3 output custom pulse CF7; =11, CF3 output custom pulse CF8;	RW	0
7:6	CF2_UDef	=00, CF2 output refers to CFCFG (bank1 60H) register definition; =01, CF2 outputs custom pulse CF6; =10, CF2 output custom pulse CF7; =11, CF2 output custom pulse CF8;	RW	0
5:4	CF1_UDef	=00, CF1 output refers to the CFCFG (bank1 60H) register definition; =01, CF1 outputs custom pulse CF6; =10, CF1 outputs custom pulse CF7; =11, CF1 output custom pulse CF8;	RW	0
3:0	D2FPREG_CFG	$\neq$ 4'b1001, the D2FP register (bank1 B0H~BBH) is used as the power channel phase segmentation calibration register; The 3-byte register high byte is invalid, but readable and writable, and the actual significant number of bits is 16 bits. =4'b1001, the D2FP register (bank1 B0H~BBH) is used as a custom power register;	RW	0

3.4.20.2. HFCONST3 Register (0x96)

Address: 96H; Word length: 2 bytes; Default: 0x0

Custom high frequency pulse constant register 3, defined below:

Bit(s)	Name	Description	R/W	Reset
15:0	HFCONST3	HFCONST3 is used for the pulse constants of 12 custom energy registers D2FE00-D2FE11 and 3 custom CF pulses CF5-CF7 when D2FCFG[3:0] equals 4'b1001; Otherwise it doesn't work. The high-frequency pulse constant register is a 2-byte unsigned number. Under the same conditions, the value obtained according to the calculation formula of HFCONST1 is used as the value of HFCONST3. The formula for calculating HFCONST1 is described in Section 3.4.1.	RW	0x0000

If the pulse constants defined by HFCONST3 and HFCOSNT1 are the same, then in the case of HFCONST3 =HFCONST1, the upper 24 bits of the 32-bit power register PT are filled with the custom power register D2FP, and the output of the custom energy pulse is consistent with the pulse output speed determined by HFCONST1.

If the defined pulse constants are different, there are two ways to adjust them, namely adjusting HFCONST3 and customizing the power register filling value. For example, the meter pulse constant defined by HFCONST1 is 1200, and the meter pulse constant defined by HFCONST3 is 24000, and the adjustment methods are as follows:

Mode 1, customize the power register $D2FP=PT/2^8$, adjust $HFCONST3=HFCOSNT1/20=HFCONST1*0.05$ accordingly;

Note: If HFCONST3 cannot obtain an integer according to the above formula, adjust the value of HFCONST1 to an integer multiple of 20 in the calibration step.

In Method 2, HFCONST3= HFCONST1, the corresponding adjustment is filled with the value filled in the custom power register, and the adjusted is:

$D2FP=PT/2^8* (24000/1200)$

3.4.20.3. D2FTIME Register (0x97)

Address: 97H; Word length: 4bytes; Default: 0x0

Custom power integration time setting register, defined as follows:

Bit(s)	Name	Description	R/W	Reset
31:14	Reserved	Reserved.	RO	0
13	D2F_START	When the register is written to 1, the hardware starts periodic timing, and when the timing time reaches the D2F_Period set time, the power value will be automatically loaded into the integrator to calculate the energy. If you want to stop counting, or need to restart counting, you need to write 0 and then 1. This register readout value is always 0. It is recommended that the software be started at the same time as the DMA waveform buffer. In this way, the period of hardware integration coincides with the cycle of the DMA waveform buffer. This register is written as 1, and the power integration time accumulation counter also clears to zero and starts counting again.	RW	0
12	D2F_MODE	=0: The integration start time is the time when the software writes the power, in the application of harmonic measurement, the software should write the harmonic power value every week, but due to the uncertainty of the software delay, the integration time cannot be guaranteed to be just a cycle; =1: The integration start time is automatically determined by the hardware, and the software only needs to ensure that the weekly wave writes the power value, which will be pre-stored in the buffer, and only when the hardware frequency interval signal comes will it be really loaded into the integrator. This scheme guarantees that the integration time of the weekly wave is accurate.	RW	0
11:0	D2F_Period	A 12-bit unsigned number that defines the time of power integration, and the minimum scale represents the sampling interval, which is defined by the DMA_WAVECON (B1 0x93) and WSAVECON (B1 0x63) registers. For example, when { DMA_WAVECON. WAVE_SR,WSAVECON. SWAVECFG,WSAVECON. When	RW	0

| | WFreqSEL } is selected as 3'b110, it represents 256 simultaneous samples, and one cycle is 256 points of sampled data. If the power calculation is calculated in units of one cycle, then this register should be written to 256-1=255 in hexadecimal 12'h0FF. This configuration represents the unit period of power integration, which is typically 20ms under normal conditions. | |

3.4.20.4. D2FP Register (0xB0~0xBB)

Address	B0H	B1H	B2H	B3H	B4H	B5H
Register	D2FP00	D2FP01	D2FP02	D2FP03	D2FP04	D2FP05
Default	0x0	0x0	0x0	0x0	0x0	0x0
Address	B6H	B7H	B8H	B9H	BAH	BBH
Register	D2FP06	D2FP07	D2FP08	D2FP09	D2FP10	D2FP11
Default	0x0	0x0	0x0	0x0	0x0	0x0

Custom power register D2FP00-11 can be in twos complement format with 24 bits with a signed number, where the highest bit is the sign bit.

When D2FCFG[3:0] is equal to 4'b1001, the register is used as 12 custom power registers, when the value is written to the register, the power will be integrated according to the pulse constant HFCONST3, and the integrated electrical energy is stored in the D2FE00~D2FE11 register, of which D2FE00, D2FE01, D2FE02 can output pulses, corresponding pulses CF5, CF6, CF7, can be based on D2FCFG [13:4] The configuration is output from the CF1~CF5 pins.

When D2FCFG[3:0] is not equal to 4'b1001, these registers are power phase calibration registers, see Section 3.4.12.

3.4.20.5. D2FE Register (0xBC~0xC7)

Address	BCH	BDH	BEH	BFH	C0H	C1H
Register	D2FE00	D2FE01	D2FE02	D2FE03	D2FE04	D2FE05
Default	0x0	0x0	0x0	0x0	0x0	0x0
Address	C2H	C3H	C4H	C5H	C6H	C7H
Register	D2FE06	D2FE07	D2FE08	D2FE09	D2FE10	D2FE11
Default	0x0	0x0	0x0	0x0	0x0	0x0

The custom energy register is a 24-bit register.

When D2FCFG[3:0] equals 4'b1001, this register corresponds one-to-one to the custom power register as one of the 12 custom energy registers. Among them, D2FE00, D2FE01, D2FE02 can output pulse CF6, CF7, CF8; It c an be selected as additive or zero-after-read type, controlled by EMUCFG.ERegCAR (B1 0x61 bit19).

These registers are meaningless when D2FCFG[3:0] is not equal to 4'b1001.

3.4.20.6.D2F_FLAG Register (0xC8)

Address: C8H; Word length: 3 bytes; Default: 0x13F

The integral circuit flag register, defined as follows:

Bit(s)	Name	Description	R/W	Reset
23:17	Reserved	Reserved.	RO	0
16	D2F_LOAD	When D2F_MODE=1 in the D2FTIME (0x1C0) register, hardware fixed time integration is used, and whenever a power value is loaded into the integrator from Buffer, the position 1 is cleared by the software write 1 to . For a typical application, the period at this position 1 is 20ms.	W1C	0
15:10	Reserved	Reserved.	RO	0
9:0	SR_TIME	A 10-bit unsigned number, read-only register representing the sampling interval of the current synchronous waveform sampling channel. 0x13F represents the current 2.048Mhz/(SR_TIME+1) = 2.048Mhz/320= 6.4Khz.	RO	0x13F

3.4.21.Sample Data Write Buffer Control Register

3.4.21.1.WSAVECON Register (0x63)

Address: 63H; Word length: 1 bytes; Default: 00H

Sampling Data Write Buffer Control Register WSAVECON controls whether ADC data for each channel is written to the buffer and how the buffer is arranged, buffer size, and waveform sampling rate are defined by the registers as follows:

Bit(s)	Name	Description	R/W	Reset
7	SWAVECFG	At DMA_WAVECON.DS_CFG=2'b00 and DMA_WAVECON.WAVE_SR=0 (B1 93H [2:0]), the data source and sample rate are jointly determined by SWAVECFG and WFreqSEL. =0, fixed sample rate mode, the WFreqSEL bit determines whether the sample rate is 6.4KHz or 7.699KHz. =1, synchronous sampling mode, the WFreqSEL bit determines whether the number of weekly synchronous sampling points is 128 points or 64 points.	RW	0
6	WFreqSEL	At DMA_WAVECON.DS_CFG=2'b00 and DMA_WAVECON.WAVE_SR=0 (bank1 93H [2:0]), the data source and sample rate are jointly determined by SWAVECFG and WFreqSEL. When SWAVECFG=0, which is fixed sample rate mode, this bit determines the fixed sample rate. =0, for fundamental frequency 50HZ sampling, 8.192MHz crystal oscillator, fixed sampling rate 6.4KHz; =1, for fundamental frequency 60Hz sampling, 8.192MHz crystal oscillator, fixed	RW	0

sampling rate 7.699KHz.

When SWAVECFG=1, which is the synchronous sampling mode, this bit determines the number of points sampled by one cycle.

=0, a fixed 128-point synchronous sampling of a cycle;

=1, a frequency fixed 64-point simultaneous sampling.

Bits	Name	Description	R/W	Reset
5:4	WSCOMM[1:0]	=2'b00 or 2'b11, do not operate; =2'b01, buffer clearing. =2'b10, configure the start waveform data write buffer according to BUFCFG[3:0]; <table><tr><td>WBUFCOM[1:0]</td><td>Command or state</td></tr><tr><td>2'b00</td><td>Writing 2'b00 is invalid and does not operate (default). When read to 2'b00, the buffer is free, or the write operation is complete and the read operation can be performed. After reset, the register is idle by default 为 2'b00</td></tr><tr><td>2'b01</td><td>Buffer zeroing command. After you configure this command for 20ms, the entire BUF is cleared.</td></tr><tr><td>2'b10</td><td>Start the waveform data write buffer as configured by BUFCFG[3:0] and DMA_WAVECON3[1].</td></tr><tr><td>2'b11</td><td>Write 2'b11 is invalid and does not operate. When read as 2'b11, it means that the buffer responds to the command, is in a write operation (zeroing or writing data), and is busy. At this time, the read operation is invalid.</td></tr></table>	RW	0
3:0	BUFCFG[3:0]	ADC Data Buffer Configuration: Work with DMA_WAVECON3 [1] to determine whether ADC data for each channel is write bufferd and the address mapping of ADC data in the buffer. This is shown in the following table.	RW	0x0

When WSCOMM[1:0] writes 2'b01, the chip responds to the clear BUF command, and the WBUFCOMM[1:0] readout value is 2'b11, indicating that the BUF starts to clear, and the chip does not respond to the new command written during the clearing process, and after 20ms, the entire BUF is cleared, and the value of WBUFCOMM[1:0] becomes 2'b00.

When WSCOMM[1:0] writes to 2'b10, the chip responds to the start buffer command, WBUFCOMM[1:0] reads the value of 2'b11, and the data begins to be written to the buffer according to the configuration of BUFCFG[3:0] and DMA_WAVECON3[1] (B1 0xE5), the chip does not respond to the new command written during the writing process, and when the buffer is total, the write is stopped, and the value of WBUFCOMM[1:0] becomes 2'b00.

Note: After the sampling frequency is adjusted, wait 2ms and then write 2'b10 to WSCOMM[1:0] to start the sampling data buffer.

After initiating the start buffer command, BUFCFG[3:0] and register bit 1 of the DMA_WAVECON3 (B1 0xE5) determine whether each channel ADC data is written to the buffer and the address mapping in the buffer. The buffer has a total of 896 address units with addresses ranging from 200H to 57FH, as shown in the following table:

Address Mapping	BANK	{DMA_WAVECON3[1], BUFCFG[3:0]}														
		5'b00000or5'b011xx	5'b00001	5'b00010	5'b00011	5'b00100	5'b00101	5'b00110	5'b00111	5'b01000	5'b01001	5'b01010	5'b01011	5'b10000	5'b10001	5'b10010
200H 27FH	B2	UA	UA	IA	UA	UB	UC								UA	UA
280H 2FFH	B2	UB	UA	IA	UA	UB	UC								UC	UB
300H 37FH	B3	UC	UB	IB	UA	UB	UC								IA	UC
380H 3FFH	B3	IA	UB	IB	IA	IB	IC	UA	UB	UC	IA	IB	IC	IN	IC	IA
400H 47FH	B4	IB	UC	IC	IA	IB	IC									IB
480H 4FFH	B4	IC	UC	IC	IA	IB	IC									IC
500H 57FH	B5															IN

Note: When DMA_WAVECON3[1] = 0, the waveform buffer area shared by the IA channel and IN channel is determined by the IN_WaveEN (94H) configuration, as detailed in the 3.4.43 IN waveform buffer enable registers section.

3.4.21.2. DMA_WAVECON Register (0x93)

Address: 93H; Word length: 4 bytes; Default: 0x0.

DMA_WAVECON configure registers for the synchronous sampling channel to supplement the WSAVECON register (bank1 63H).

Bit(s)	Name	Description	R/W	Reset
31:14	Reserved	Reserved.	RO	0
13:4	WAVECNT	Used to change the sample rate of the bufferd waveform: If the desired number of frequency sampling points is N, configure it as follows: WAVECNT=((2.048*10^6)/freq/N)-1 (freq is the grid frequency, generally 50Hz or 60Hz) (N is the sample rate configured by WAVE_SR, such as 64/128/256/512) When WAVECNT≠0 is configured, WAVECNT remains unchanged during the waveform buffering process, and the WAVECNT value is used to participate in the calculation when calculating checksum. The minimum supported write value at this point is 64. When the value written is less than 64, the expected value can be written, but the actual effect has always been 63 (i.e., the sample rate has always been fixed at 32Khz, and the maximum only supports 32KHz). When WAVECNT=0 is configured, WAVECNT will change according to the actual sampling divider during the waveform caching process, reflecting the actual sampling divider. But does not participate in checksum calculations; That is, the read value of the register bit is ignored when checksum is calculated, and the checksum is always calculated with WAVECNT=0. When WAVECNT is reset at power-on, WAVECNT=0 is configured by default, and the actual sampling divider of WAVECNT reacts, so its power-on default is changing.	RW	---
3	WAVE_DIV	1/2 of the number of simultaneous sampling points is decimated for waveform buffer. =0, not decimate; =1, 1/2 of the decimated are wrote into RAM For example: The waveform buffer requires 64 points/cycle of data, and the half-cycle RMS requires 64 points/half-cycle data. The simultaneous sampling channel can then be configured for simultaneous sampling of 128 points/frequency and this bit can be enabled.	RW	0
2	WAVE_SR	=0, determined by the SWAVECFG and WFreqSEL of the WSAVECON register. SWAVECFG=1,WFreqSEL=0: Simultaneous 128-point sampling; SWAVECFG=1,WFreqSEL=1: Simultaneous 64-point sampling; =1, determined jointly by SWAVECFG and WFreqSEL of the WSAVECON register.	RW	0

		SWAVECFG=1,WFreqSEL=0: Simultaneous 256-point sampling; SWAVECFG=1,WFreqSEL=1: Simultaneous 512-point sampling;		
1:0	DS_CFG1	=2'b00: Select the waveform for synchronous frequency tracking, and the number of sampling points is determined by BIT[13:2]; =2'b01: Select the data before the EMU channel gain and channel phase calibration [7:0], high-pass filter; Fixed 8k sampling, which is affected by DC offset calibration; =2'b10: Select the data after EMU channel gain and channel phase calibration, DC offset calibration, and high-pass filter; (DC calibration is not performed by default, high-pass filter is on), fixed 8K sampling rate; =3'b11: Select the fundamental data after EMU channel gain and channel phase calibration, DC offset calibration, and high-pass filter; (DC calibration is not performed by default, high-pass filter is on), fixed 8K sampling rate;	RW	0

3.4.21.3. DMA_WAVECON3 Register (0xE5)

Address: E5H; Word length: 4 bytes; Default: 0x0

DMA_WAVECON3 is configuration register 3 for the synchronous sampling channel to supplement the waveform buffer storage format.

Bit(s)	Name	Description	R/W	Reset
31:12	Reserved	Reserved	RO	0
11	SPI_INV	SPI reads waveform data in reverse byte order: =0: The SPI readout waveform data sequence is data[23:16]→data[15:8]→data[7:0]; =1: The SPI readout waveform data sequence is data[7:0]→data[15:8]→data[23:16];	RW	0
10	Bufcfg	Channel buffer mode selection: =0: channel chunked buffer mode; =1: channel cross-buffer mode; (See Section 6.2 for details)	RW	0
9:2	Cont_N	Number of consecutive waveform buffer =0, and Cont_en=0, by WSAVECON. WSCOMM[1:0] decides on single-shot buffer mode (mode 0); Cont_en=1, continuous unlimited buffer mode (mode 2).	RW	0

			=N, and Cont_en=0, by WSAVECON. WSCOMM[1:0] decides on single-shot buffer mode (mode 0); Cont_en=1, continuous limited number of times buffer mode (mode 1), the number of times is N.		
1	BUFCFG[4]		Determine the waveform buffer storage format with WSAVECON register BUFCFG [3:0].	RW	0
0	Cont_en		=0 to stop continuous buffering. =1 to start continuous buffering.	RW	0

3.4.22.Synchronous sampling channel calibration register

3.4.22.1.DMA_WAVECON2 Register (0xD1)

Address: 0xD1; Default: 0x3F800

DMA_WAVECON2 is configuration register 2 for the synchronous sampling channel for configuration related to synchronous sampling channel calibration.

Bit(s)	Name	Description	R/W	Reset
31:19	Reserved	Reserved	RO	0
18	HW_CLASS	=0, repeat the half-cycle wave sliding window, and the half-cycle wave updates the one-week wave mean root value. (pseudo-A level) =1, no duplicate data sliding window, the HWCNT register manually configures the number of points, and the software decides whether to slide the half-cycle or one-week wave. Includes: Weekly Mean Square Root Value (Standard S Class) or Half Cycle Root Value (Old Standard) with Half Cycle Update (Old Standard)	RW	0
17:11	DCOS_CHX_CHKEN	BIT [17:11] corresponds {DCOS_IN , DCOS_UC , DCOS_UB , DCOS_UA , DCOS_IC , DCOS_IB , DCOS_IA} =0 , DCOS_XX register does not participate in the configuration register checksum calculation; =1 , DCOS_XX register participate in the configuration register checksum calculation.	RW	0x7F
10	CIC_AAC_EN	=0: Harmonic attenuation compensation function is not enabled; =1: Enable harmonic attenuation compensation function; When this function is enabled, there is no longer a need to compensate for harmonic coefficients when reading DMA waveform buffer for FFT.	RW	0
09	CIC_AGC_EN	=0: The gain auto-adjustment function of the DMA	RW	0

		waveform buffer channel is not enabled; =1: Enable the gain auto-adjustment function of the DMA waveform buffer channel; The gain auto-adjustment function is to solve the gain change caused by the change in power frequency during synchronous sampling. After this function is enabled, the gain adjustment is no longer needed, and the waveform amplitude obtained by the DMA waveform channel will be consistent with the instantaneous waveform amplitude of the metering channel (the instantaneous waveform sampling register (00H~06H) of the metering channel 8KHz).		
08	CIC_DC_EN	=0: Channel DC OFFSET calibration register DCOSx (1AH~20H) does not participate in DC OFFSET calibration of DMA synchronous sampling channel; =1: Channel DC OFFSET calibration register DCOSx (1AH~20H) participates in DC OFFSET calibration of DMA synchronous sampling channel;	RW	0
07	Reserved	Reserved	RO	0
06:00	WAVE_HPFOFF	DMA Waveform channel high-pass filter switch, =0, enable the high-pass filter, enable the high-pass filter by default; It is recommended to enable the high-pass filter。 =1，turn off high-pass filter. The specific definition is as follows: WAVE_HPFOFF[6]HPFOFF_IN_WAVE WAVE_HPFOFF[5]HPFOFF_IC_WAVE WAVE_HPFOFF[4]HPFOFF_IB_WAVE WAVE_HPFOFF[3]HPFOFF_IA_WAVE WAVE_HPFOFF[2]HPFOFF_UC_WAVE WAVE_HPFOFF[1]HPFOFF_UB_WAVE WAVE_HPFOFF[0]HPFOFF_UA_WAVE Note: It is recommended that in NVM1 mode, instead of using this set of register bits to turn off high-pass filter, use NVM1CFG.bit1 to turn off high-pass filter.	RW	0

3.4.22.2. DMA_PHS_WAVE Register (0xD2~0xD8)

Address	D2H	D3H	D4H	D5H	D6H	D7H	D8H
Register	PHS_UA_WAVE	PHS_UB_WAVE	PHS_UC_WAVE	PHS_IA_WAVE	PHS_IB_WAVE	PHS_IC_WAVE	PHS_IN_WAVE
Default	0x0	0x0	0x0	0x0	0x0	0x0	0x0

The above phase calibration register can complete the phase calibration of the waveform buffer channel, and the calibration principle is the same as PHSU/I (0x0C~0x12, channel phase calibration register).

The actual number of significant digits of PHS_IA_WAVE/PHS_IB_WAVE /PHS_IC_WAVE /PHS_IN_WAVE /PHS_UA_WAVE /PHS_UB_WAVE /PHS_UC_WAVE is 10 digits.

There are two levels of phase calibration:

The first stage is the one-bit data flow calibration of the ADC, the sampling rate is fixed at 2.048Mhz, the resolution changes with the change of power frequency, taking 50Hz as an example, the calculation formula: $360/(2.048*10^6/50)=0.008789°$.

The DMA_PHS_WAVE [6:0] of each register supports the first level of calibration, the calibration range of the first stage is set to 360 degrees / 256 point sampling / 2 = 0.7 degrees or so, the actual maximum supported calibration value is 87 (decimal, the maximum phase shift is $87 * 0.008789 = 0.7646°$), when the value written by DMA_PHS_WAVE [6:0] is greater than 87, it is processed according to 87.

The first stage calibration is exactly the same as the calibration principle of the metering channel, and if the first-stage calibration range can meet the application requirements, these registers can fill in the same offset calibration value as the metering channel (note that the metering channel is offset on a 0x80 basis)。

The second stage of phase calibration is to cope with the current transformer in some special occasions, which have a large phase delay and need to support the phase calibration with a larger delay.

The second stage calibration is the sine wave delay phase calibration after the CIC decimation filter, which is different from the metering channel fixed sampling rate (8Khz), if synchronous sampling is configured, the phase scale represented by moving a sample point is fixed (such as 256 points synchronous sampling, moving a sampling point phase shift fixed to 360/256=1.40625 degrees), practical application needs to pay attention to this problem。

The second level of calibration only considers the case of 256 points of simultaneous sampling, and a total o f 3 bits are set for phase calibration DMA_PHS_WAVE [9:7], which is defined as follows:

DMA_PHS_WAVE [9:7]=3'b000: represents that there is no delay after CIC filtering

DMA_PHS_WAVE [9:7]=3'b001: represents delay 360°/ 256 points = 1.40625°

DMA_PHS_WAVE [9:7]=3'b010represents delay 2*360°/256 points=2.8125°

DMA_PHS_WAVE [9:7]=3'b011represents delay 3*360°/256 points=4.21875°

DMA_PHS_WAVE [9:7]=3'b100represents delay 4*360°/256 points=5.625°

DMA_PHS_WAVE [9:7]=others, reserved bit, not allowed to fill in (if filled, the effect is equivalent to 3'b000)

DMA_PHS_WAVE [9:7] and DMA_PHS_WAVE [6:0] together can achieve phase adjustment in the range of 0~6.325°.

If the number of simultaneous sampling points set is not 256 points, the above formula needs to be adjusted accordingly.

3.4.22.3. DMA_GS_WAVE Register (0xD9~0xDF)

Address	D9H	DAH	DBH	DCH	DDH	DEH	DFH
Register	GSUA_WAVE	GSUB_WAVE	GSUC_WAVE	GSIA_WAVE	GSIB_WAVE	GSIC_WAVE	GSIN_WAVE
Default	0x0	0x0	0x0	0x0	0x0	0x0	0x0

These registers are used to synchronize the gain calibration of the sampling channel. The gain register is a 2-byte signed number in twos complement form, with the highest bit being the sign bit, indicating the range (-1, +1).

Calibration formula:

If RegGain>=2^{15}, then *Gain=(RegGain-2^{16})/2^{15}*; otherwise *Gain=RegGain/2^{15}*;

Where RegGain is channel gain register.

Taking the IB channel as an example, assume that the RMS of the B channel current IB before calibration and IB' after calibration are the relationship between the two is: *IB'=IB+IB*Gain*

Note that the formula valid range ensures that the signal is still within the ADC total-scale range after multiplying the channel gain.

3.4.23. Half-cycle RMS Configuration Register 2 (0xE6)

Address: E6H; Word length: 4 bytes; Default: 0x3F

The synchronous sampling channel half-cycle RMS configuration register 2---HWCNT, is defined as follows:

Bit(s)	Name	Description	R/W	Reset
31:9	Reserved	Reserved	RO	0
8:0	HW_CNT	For simultaneous sampling channel half-cycle RMS 2 squared accumulation calculation: If the desired square sum points is N, then HW_CNT=N-1; N can be the number of total-cycle sampling points or half-cycle sampling points, and the software determines the half-cycle RMS calculation mode.	RW	0x3F

3.4.24. Rogowski coil sensor Configuration Registers ROS_CFG (0xE6)

Address: EDH; Word length: 4 bytes; Default: 0x0.

This register is enabled by WREN2 writes and participates in CHECKSUM3 verification. The procedure for using Rogowski coil sensor can be found in the *Rogowski coil sensor Application Note*.

Bit(s)	Name	Description	R/W	Reset
31:4	Reserved	Reserved	RO	0
3	ROS_IN_EN	=0, select to turn off the Rogowski coil sensor function of the IN current channel; =1, select the Rogowski coil sensor function that enables the IN current channel;	RW	0
2	ROS_IC_EN	=0, select to turn off the Rogowski coil sensor function of the IC current channel; =1, select the Rogowski coil sensor function that enables the IC current channel;	RW	0
1	ROS_IB_EN	=0, choose to turn off the Rogowski coil sensor function of the IB current channel; =1, select the Rogowski coil sensor function that	RW	0

		enables the IB current channel;		
0	ROS_IA_EN	=0, select to turn off the Rogowski coil sensor function of the IA current channel; =1, select the Rogowski coil sensor function that enables the IA current channel;	RW	0

3.4.25.Rogowski coil sensor Integral DC Attenuation Factor Register ROS_DCATTC (0xEB)

Address: EBH; Word length: 4 bytes; Default: 0x0.

This register is enabled by WREN2 writes and participates in CHECKSUM3 verification.

Bit(s)	Name	Description	R/W	Reset
31:16	Reserved	Reserved	RO	0
15:0	DC_ATTC	This register is only valid when Rogowski coil sensor integration is enabled (ROS_CFG[3:0]), 2 bytes are valid, and bit15 is a sign bit but fixed at 0. For the use of Rogowski coil sensor s, see *Roche Coils Application Note*	RW	0x0

3.4.26.Rogowski coil sensor Integral Conversion Factor Register ROS_Tran_K (0xEC)

Address: ECH; Word length: 4bytes; Default: 0x507.

This register is WREN2 write enabled and does not participate in validation.

Bit(s)	Name	Description	R/W	Reset
31:16	Reserved	Reserved	RO	0
15:0	Tran_K	This register is only valid when Rogowski coil sensor integration is enabled (ROS_CFG[3:0]). For the use of Rogowski coil sensor s, see *Roche Coils Application Note*.	RW	0x507

3.4.27.Metrology Interrupt Register

3.4.27.1.EMMIE Register (0x64)

Address: 64H; Word length: 2 bytes; Default: 0000H

This register is the interrupt enable register in EMM mode. Under EMM, the corresponding interrupt allowable bit is configured to 1 and the IF clears, and when this event occurs, the INTN pin outputs a low level.

Bit(s)	Name	Description
15	OVIIE	Overvoltage overcurrent interrupt enabled. =1, enabled. =0, not allowed. The default is 0, the same below.

14	SAGIE	Voltage sag interrupt enable.
13	IRegion3IE	Current segmented state change interrupts enable.
12	Reserved	Reserved
11	CF4IE	CF4 pulse output interrupt enable.
10	CF3IE	CF3 pulse output interrupt enable.
9	CF2IE	CF2 pulse output interrupt enable.
8	CF1IE	CF1 pulse output interrupt enable.
7	ZXINIE	Channel IN positive zero-crossing interrupt enable.
6	ZXICIE	Channel IC positive zero-crossing interrupt enable.
5	ZXIBIE	Channel IB positive zero-crossing interrupt enable.
4	ZXIAIE	Channel IA positive zero-crossing interrupt enable.
3	ZXUCIE	Channel UC positive zero-crossing interrupt enable.
2	ZXUBIE	Channel UB positive zero-crossing interrupt enable.
1	ZXUAIE	Channel UA positive zero-crossing interrupt enable.
0	WAVUDIE	Sampled waveform interrupt enable.

3.4.27.2. EMMIF Register (0x65)

Address: 65H; Word length: 2 bytes

This register is the event status register in EMM mode. Under EMM, when an event occurs, the corresponding IF position 1. When the corresponding interrupt allowable bit is configured to 1, state position 1 causes the INT pin output to go low.

Bit(s)	Name	Description
15	OVIIF	Overvoltage overcurrent interrupt flag. This position 1 occurs when overvoltage occurs in any phase of the polyphase voltage, or when overcurrent occurs in any phase of the polyphase current. If the OVIE interrupt is enabled, =1 causes the INT pin to flip from high to low. This bit is written to zero 1 while clearing interrupts and clearing the OVUA, OVUB, OVUC, OIIA, OIIB, OIIC status flag bits in the PHASES status register.
14	SAGIF	Voltage sag interrupt flag. When bit 15 in EMUCFG is 1: the polyphase voltage dips at the same time, and this position is 1. When bit 15 in EMUCFG is 0: position 1 when any of the three phases of voltage

		dips.
		If the SAGIE interrupt is enabled, =1 causes the INT pin to flip from high to low.
		This bit is written 1 and clear while clearing the interrupt and PHASES status register of the SAGUA, SAGUB, SAGUC status flags.
13	IRegion3IF	Current segment 3 segment state change flag.
		Three-phase four-wire: This position 1 occurs when the RMS of the A/B/C polyphase either phase current changes relative to the segmented state set by IRegion3H/IRegion3L.
		Three-phase three-wire: position 1 when the RMS current of either phase of A/C changes relative to the segmented state of the IRegion3H/IRegion3L setting.
		The IregionS register can be further queried to confirm which phase current RMS segment status changes.
		If IRegion3 interrupt is enabled, =1 causes the INTN pin to flip from high to low.
		This bit writes 1 and clear, and if IRegion3IE=1, it clears and interrupts.
12	Reserved	Reserved
11	CF4IF	CF4 pulse output flag. Write 1 to and clear. If CF4IE=1, clear and clear interrupt at the same time.
10	CF3IF	CF3 pulse output flag. Write 1 to and clear. If CF3IE=1, clear and clear interrupt at the same time.
9	CF2IF	CF2 pulse output flag. Write 1 to and clear. If CF2IE=1, clear and clear interrupt at the same time.
8	CF1IF	CF1 pulse output flag. Write 1 to and clear. If CF1IE=1, clear and clear interrupt at the same time.
7	ZXINIF	Channel IN positive zero-crossing flag. Write 1 to and clear. If ZXINIE=1, clear and clear the interrupt at the same time.
6	ZXICIF	Channel IC positive zero-crossing flag. Write 1 to and clear. If ZXICIE=1, clear and clear the interrupt at the same time.
5	ZXIBIF	Channel IB positive zero-crossing flag. Write 1 to and clear. If ZXIBIE=1, clear and clear the interrupt at the same time.
4	ZXIAIF	Channel IA positive zero-crossing flag. Write 1 to and clear. If ZXIAIE=1, clear and clear the interrupt at the same time.
3	ZXUCIF	Channel UC positive zero-crossing flag. Write 1 to and clear. If ZXUCIE=1, clear and clear the interrupt at the same time.
2	ZXUBIF	Channel UB positive zero-crossing flag. Write 1 to and clear. If ZXUBIE=1, clear and clear the interrupt at the same time.
1	ZXUAIF	Channel UA positive zero-crossing flag. Write 1 to and clear. If ZXUAIE=1, clear and clear the interrupt at the same time.

0	WAVUDIF	Waveform sampling flag. 1/2/4/8Khz selectable rate refresh, determined by EMUCFG3.WAVUDCFG. Write 1 to zero. If WAVUDIE=1, clear and clear the interrupt at the same time.		

3.4.27.3.EMMIE2 Register (0x6B)

Address: 6BH; Default: 0x0

This register is the EMU interrupt 2 enable register. When the corresponding interrupt allowable bit is configured to 1 and the IF is cleared, when the event occurs, the corresponding EMMIF2 position bit and generate EMU interrupt 2.

Bit(s)	Name	Description	R/W	Reset
31:28	Reserved	Reserved	RO	0
27	ECT_INTSEL	=0, ECT block error out-of-bounds error interrupt and gain factor update interrupt select INTN1 output; =1, ECT block error out-of-bounds error interrupt and gain factor update interrupt select INTN2 output.	RW	0
26	HW_INTSEL	=0, half-cycle RMS 2 update interrupt selects INTN1 output; =1, half-cycle RMS 2 updates the interrupt to select the INTN2 output.	RW	0
25	LVD_INTSEL	=0, LVD interrupt selects INTN1 output; =1, LVD interrupt selects the INTN2 output.	RW	0
24	HW_RMS_IE	Simultaneous sampling half-cycle RMS 2 update interrupt enable	RW	0
23	AUTOECT_ERREL_IE	ECT module error out-of-bounds error interrupt	RW	0
22	AUTOECT_GAINUDIE	ECT block gain factor update interrupt	RW	0
21	FLK_INTSEL	=0, FLK interrupt and FLK error interrupt select INTN1 output; =1, FLK interrupt and FLK error interrupt select INTN2 output.	RW	0
20	HSDC_INTSEL	=0, HSDC interrupt and HSDC error interrupt select INTN1 output; =1, HSDC interrupt and HSDC error interrupt select INTN2 output.	RW	0
19	WAVE_INTSEL	=0, waveform buffer total/half total interrupt selects the INTN1 output; =1, waveform buffer total/half-total interrupt selects the INTN2 output.	RW	0

18	SAG_INTSEL	=0, UA/UB/UC SAG interrupt selects INTN1 output; =1, UA/UB/UC SAG interrupts select the INTN2 output.	RW	0
17	OV_INTSEL	=0, overvoltage OVA/OVB/OVC events select INTN1 output; =1, overvoltage OVA/OVB/OVC events select INTN2 output.	RW	0
16	OI2_INTSEL	=0, overcurrent OIA2/OIB2/OIC2 events select INTN1 output; =1, overcurrent OIA2/OIB2/OIC2 events select INTN2 output.	RW	0
15	LVD_IE	LVD events generate interrupt enable	RW	0
14	FLK_ERR_IE	The flicker module outputs error interrupt enable	RW	0
13	FLK_IE	The flicker module interrupt enable	RW	0
12	HSDC_ERR_IE	HSDC outputs error interrupt enable	RW	0
11	HSDC_TWAVE_HIE	HSDC output waveform buffer half-block interrupt enable	RW	0
10	WAVE_FIE	Waveform buffer total interrupt enable	RW	0
9	WAVE_HFIE	Waveform buffer half-total interrupt enable	RW	0
8	UC_SAGIE	C-phase voltage sag interrupt enable	RW	0
7	UB_SAGIE	B-phase voltage sag interrupt enable	RW	0
6	UA_SAGIE	A-phase voltage sag interrupt enable	RW	0
5	OVC_IE	C-phase overvoltage interrupt enable	RW	0
4	OVB_IE	B-phase overvoltage interrupt enable	RW	0
3	OVA_IE	A-phase overvoltage interrupt enable	RW	0
2	OIC2_IE	C-phase overcurrent interrupt enable	RW	0
1	OIB2_IE	B-phase overcurrent interrupt enable	RW	0
0	OIA2_IE	A-phase overcurrent interrupt enable	RW	0

Note: The voltage overvoltage and current overcurrent interrupts in EMU Interrupt 2 and the overvoltage/overcurrent interrupts in EMU Interrupt 1 can be set and generated independently.

3.4.27.4.EMMIF2 Register (0x6C)

Address: 6CH;

This register is the EMU interrupt 2 status register. When an event occurs in EMU interrupt 2, the corresponding IF position 1. When the corresponding interrupt allowable bit is configured to 1, state position 1 generates an EMU interrupt 2.

Bit(s)	Name	Description	R/W	Reset
31:24	Reserved	Reserved	RO	0
23	AUTOECT_ERREL_IF	ECT module error out-of-bounds error interrupt flag, clear automatic temperature compensation error out-of-bounds flag, that is, to the ECT_CMD_STATUS. [19:13] Write 7'h7F, clear the flag.	RO	0
22	AUTOECT_GAINUD_IF	ECT module gain factor updates interrupt flag, and the automatic temperature compensation temperature out-of-bounds event flag is cleared, that is, to the ECT_CMD_STATUS. [10:4] Write 7'h7F, clear the flag.	RO	0
21	Reserved	Reserved	RO	0
20	HSDC_BUSY	HSDC waveform output busy flag (HSDC_BUSY=1, it is recommended not to turn off the HSDC_EN enable, HSDC_EN=0 this flag is set to 0)	RO	0
19	HW_ZXIN	IN channel half-cycle RMS update flag, configuration EMU_CFG. FREQ_SEL=0, that is, the update time is 10ms when 50Hz is applied, and the configuration is EMU_CFG. FREQ_SEL=1, that is, the update time is 8.3333ms when applying 60Hz, write 1 to and clear 0.	W1C	0
18	HW_ZXUC	UC channel half-cycle RMS update flag, configuration EMU_CFG. FREQ_SEL=0, that is, the update time is 10ms when 50Hz is applied, and the configuration is EMU_CFG. FREQ_SEL=1, that is, the update time is 8.3333ms when 60Hz is applied, write 1 to and clear 0.	W1C	0
17	HW_ZXUB	UB channel half-cycle RMS update flag, configuration EMU_CFG. FREQ_SEL=0, that is, the update time is 10ms when 50Hz is applied, and the configuration is EMU_CFG. FREQ_SEL=1, that is, the update time is 8.3333ms when 60Hz is applied, write 1 to and clear 0.	W1C	0
16	HW_ZXUA	UA channel half-cycle RMS update flag, configuration EMU_CFG. FREQ_SEL=0, that is,	W1C	0

		the update time is 10ms when 50Hz is applied, and the configuration is EMU_CFG. FREQ_SEL=1, that is, the update time is 8.3333ms when 60Hz is applied, write 1 to and clear 0.		
15	LVD_IF	LVD events generate interrupt flag.	W1C	0
14	FLK_ERR_IF	The flicker module outputs an error interrupt enabled, and when the FLK data is overwritten during SPI reading FLK_FIFO, FLK_ERR=1. If the corresponding interrupt is enabled, the output is interrupted, write 1 to clear 0 and clear interrupt.	W1C	0
13	FLK_IF	=0:10ms 5 times flicker module calculation is not completed, 10ms FLK data FIFO is not total; =1: 10ms 5 times the flicker module calculation is completed, and the 10ms FLK data FIFO is total. The flag bit writes 1 to clear 0 and clear the interrupt, and whether the flag bit is generated by FLK_IE has nothing to do with it. If the corresponding interrupt is enabled, the output is interrupted, write 1 to clear 0.	W1C	0
12	HSDC_ERR_IF	HSDC outputs an error interrupt flag, HSDC_ERR_IF=1 when the waveform buffer half total flag is received again during HSDC waveform output. If the corresponding interrupt is enabled, the output is interrupted, write 1 to clear 0 and clear interrupt.	W1C	0
11	HSDC_TWAVE_HIF	HSDC outputs waveform buffer half-block interrupt flag, writes 1 clear 0 and clear interrupt.	W1C	0
10	WAVE_FIF	Waveform buffer total flag, write 1 to clear 0 and clear interrupt.	W1C	0
9	WAVE_HFIF	Waveform buffer half-total flag, write 1 to clear 0 and clear interrupt.	W1C	0
8	UC_SAGIF	C-phase voltage sag interrupt flag If UC_SAGIE enables the interrupt，=1 will generate EMU interrupt. This bit writes 1 to clear 0 and clears interrupts, but does not clear the SAGUC status flag bit in the PHASES status register.	W1C	0
7	UB_SAGIF	B-phase voltage sag interrupt flag If UB_SAGIE enables the interrupt，=1 will generate EMU interrupt.	W1C	0

		This bit writes 1 to clear 0 and clears interrupts, but does not clear the SAGUB status flag bit in the PHASES status register.		
6	UA_SAGIF	A-phase voltage sag interrupt flag	W1C	0
		If UA_SAGIE enables the interrupt，=1 will generate EMU interrupt.		
		This bit writes 1 to clear 0 and clears interrupts, but does not clear the SAGUA status flag bit in the PHASES status register.		
5	OVC_IF	C-phase overvoltage output flag.	W1C	0
		If OVC_IE = 1, OVC_IF asserting causes an overvoltage interrupt in C-phase.		
		OVC_IF write 1 to clear 0 and clear interrupt at the same time.		
4	OVB_IF	B-phase overvoltage output flag.	W1C	0
		If OVB_IE = 1, OVB_IF asserting causes an overvoltage interrupt in B-phase.		
		OVB_IF write 1 to clear 0 and clear interrupt at the same time.		
3	OVA_IF	A-phase overvoltage output flag.	W1C	0
		If OVA_IE = 1, OVA_IF asserting causes an overvoltage interrupt in A-phase.		
		OVA_IF write 1 to clear 0 and clear interrupt at the same time.		
2	OIC2_IF	C-phase overcurrent flag.	W1C	0
		If OIC2_IE=1, the OIC2_IF assertion causes an overcurrent break in the C phase.		
		OIC2_IF write 1 to clear 0 and clear interrupt at the same time.		
1	OIB2_IF	B-phase overcurrent flag.	W1C	0
		If OIB2_IE=1, the OIB2_IF assertion causes an overcurrent break in the B phase.		
		OIB2_IF write 1 to clear 0 and clear interrupt at the same time.		

		A-phase overcurrent flag.		
0	OIA2_IF	If OIA2_IE=1, the OIA2_IF assertion causes an overcurrent break in the A phase.	W1C	0
		OIA2_IF write 1 to clear 0 and clear interrupt at the same time.		

Note: The voltage overvoltage and current overcurrent interrupts in EMU Interrupt 2 and the overvoltage/overcurrent interrupts in EMU Interrupt 1 can be set and generated independently.

3.4.28.Power Direction Register PQSign (0x66)

Address: 66H; Word length: 2 bytes

The PQSign register is a total active/total reactive/fundamental active/fundamental reactive direction register. The direction is based on the average power symbol of each phase and the conjunction, and is updated synchronously with the average power register, and the update period is 250ms.

Bit(s)	Name	Description	R/W	Reset
15	FQTSIGN	=0, indicates that the fundamental all-phase reactive power sign is +; =1 indicates that the fundamental all-phase reactive power symbol is -.	RO	0
14	FQCSIGN	=0, indicates that the fundamental C-phase reactive power sign is +; =1 indicates that the fundamental C-phase reactive power symbol is -.	RO	0
13	FQBSIGN	=0, indicates that the fundamental B-phase reactive power sign is +; =1 indicates that the fundamental B-phase reactive power symbol is -.	RO	0
12	FQASIGN	=0, indicates that the fundamental A-phase reactive power sign is +; =1 indicates that the fundamental A-phase reactive power symbol is -.	RO	0
11	FPTSIGN	=0, indicates that the fundamental all-phase active power sign is +; =1 indicates that the fundamental all-phase active power symbol is -.	RO	0
10	FPCSIGN	=0, indicates that the fundamental C-phase active power sign is +; =1 indicates that the fundamental C-phase active power symbol is -.	RO	0
9	FPBSIGN	=0, indicates that the fundamental B-phase active power sign is +; =1 indicates that the fundamental B-phase active power symbol is -.	RO	0
8	FPASIGN	=0, indicates that the fundamental A-phase active power sign is +; =1 indicates that the fundamental A-phase active power symbol is -.	RO	0
7	QTSIGN	=0, indicates that the all-phase reactive symbol is +; =1 indicates that the all-phase reactive symbol is -.	RO	0

6	QCSIGN	=0, indicates that the C-phase reactive symbol is +; =1 indicates that the C-phase reactive symbol is -.	RO	0
5	QBSIGN	=0, indicates that the B-phase reactive symbol is +; =1 indicates that the B-phase reactive symbol is -.	RO	0
4	QASIGN	=0, indicates that the A-phase reactive symbol is +; =1 indicates that the A-phase reactive symbol is -.	RO	0
3	PTSIGN	=0, indicates that the all-phase active symbol is +; =1 indicates that the all-phase active symbol is -.	RO	0
2	PCSIGN	=0, indicates that the C-phase active symbol is +; =1 indicates that the C-phase active symbol is -.	RO	0
1	PBSIGN	=0, indicates that the B-phase active symbol is +; =1 indicates that the B-phase active symbol is -.	RO	0
0	PASIGN	=0, indicates that the A-phase active symbol is +; =1 indicates that the A-phase active symbol is -.	RO	0

3.4.29. No-load Status Flag Register Noload (0x67)

Address: 67H; Word length: 2bytes

The Noload register represents the phase-wide active apparent / total reactive / fundamental active apparent / fundamental reactive latent state. This register is used with the IStart_PS, IStart_Q register, and register bit NoLoadCFG (EMUCFG.16). This register update cycle is 250ms.

Bit(s)	Name	Description	R/W	Reset
15	Reserved	Reserved	RO	0
14	FNoQldC	=0, indicates that the fundamental C-phase reactive is not in no-load status; =1 indicates that the fundamental C-phase reactive power is in no-load status.	RO	0
13	FNoQldB	=0, indicates that the fundamental B-phase reactive is not in no-load status; =1 indicates that the fundamental B-phase reactive power is in no-load status.	RO	0
12	FNoQldA	=0, indicates that the fundamental A-phase reactive is not in no-load status; =1 indicates that the fundamental A-phase reactive power is in no-load status.	RO	0
11	Reserved	Reserved	RO	0
10	FNoPSldC	=0, indicates that the fundamental C-phase active and the apparent is not in no-load status; =1, indicates that the fundamental C-phase active and apparent is in no-load status.	RO	0
9	FNoPSldB	=0, indicates that the fundamental B-phase active and the apparent is not in no-load status; =1, indicates that the	RO	0

Bit(s)	Name	Description	R/W	Reset
		fundamental B-phase active and apparent is in no-load status.		
8	FNoPSldA	=0, indicates that the fundamental A-phase active and the apparent is not in no-load status; =1, indicates that the fundamental A-phase active and apparent is in no-load status.	RO	0
7	Reserved	Reserved	RO	0
6	NoQldC	=0, indicates that the fundamental C-phase reactive is not in no-load status; =1, indicates that the fundamental C-phase reactive is in no-load status.	RO	0
5	NoQldB	=0, indicates that the fundamental B-phase reactive is not in no-load status; =1, indicates that the fundamental B-phase reactive is in no-load status.	RO	0
4	NoQldA	=0, indicates that the fundamental A-phase reactive is not in no-load status; =1, indicates that the fundamental A-phase reactive is in no-load status.	RO	0
3	Reserved	Reserved	RO	0
2	NoPSldC	=0, indicates that the C-phase active and the apparent is not in no-load status; =1, indicates that the C-phase active and apparent is in no-load status.	RO	0
1	NoPSldB	=0, indicates that the C-phase active and the apparent is not in no-load status; =1, indicates that the C-phase active and apparent is in no-load status.	RO	0
0	NoPSldA	=0, indicates that the C-phase active and the apparent is not in no-load status; =1, indicates that the C-phase active and apparent is in no-load status.	RO	0

3.4.30.Current Segment Status Register IRegionS (0x68)

Address: 68H, Word length: 1 byte

The IRegionS register indicates the segment status of each per-phase currents. This register combines with the current segment region setting register IRegionL and IRegionH, as well as IRegionIE and IRegionIF. The update cycle of this register is 250ms.

Bit(s)	Name	Description	R/W	Reset
7:3	Reserved	Reserved	RO	0
2	Iregion3SC	= 0, phase C current RMS is in the segment region 1. = 1, phase C current RMS is in the segment region 2.	RO	0
1	Iregion3SB	= 0, phase B current RMS is in the segment region 1. = 1, phase B current RMS is in the segment region 2.	RO	0

	Iregion3SA	= 0, phase A current RMS is in the segment region 1.	RO	0
0		= 1, phase A current RMS is in the segment region 2.		

3.4.31.Phase Voltage and Current Status Register PHASES (0x69)

Address: 69H, Length: One byte

The PHASES register indicates the status of the phase loss of voltage, phase sequence error, voltage sag, overvoltage, and the phase overcurrent status. This register combines with the register and register bit LostVoltage, MODSEL (three-phase four-wire and three-phase three-wire voltage sequence error criterion are different), SAGCFG, OVLVL, OILVL, SAGIE, SAGIF, OVIIE and OVIIF.

Bit(s)	Name	Description	R/W	Reset
15	Reserved	Reserved	RO	0
14	OIIC	= 0, IC is not overcurrent. = 1, IC is overcurrent. When write 1 to clear OVIIF, it will clear this bit simultaneously.The same as OIIB,OIIA,OVUC,OVUB,OVUA.	RO	0
13	OIIB	= 0, IB is not overcurrent. = 1, IB is overcurrent.	RO	0
12	OIIA	= 0, IA is not overcurrent. = 1, IA is overcurrent.	RO	0
11	Reserved	Reserved	RO	0
10	OVUC	= 0, UC is not overvoltage. = 1, UC is overvoltage.	RO	0
9	OVUB	= 0, UB is overvoltage. = 1, UB is not overvoltage.	RO	0
8	OVUA	= 0, UA is overvoltage. = 1, UA is not overvoltage.	RO	0
7	Reserved	Reserved	RO	0
6	SAGUC	= 0, UC is not voltage sag. = 1,UC is voltage sag. When write 1 to clear SAGIF, it will clear this bit simultaneously.The same as SAGUB,SAGUA.	RO	0
5	SAGUB	= 0, UB is not voltage sag.	RO	0

		= 1, UB is voltage sag.		
4	SAGUA	= 0,UA is not voltage sag. = 1,UA is voltage sag.	RO	0
3	UPhSqErr	= 0, voltage phase sequence is normal. = 1,voltage phase sequence is error. Criterion of Three-phase four-wire: ① YUBUA is out of 120°±10°, ② YUCUA is out of 240°±10°, ③ UA < ZXOT (normalized value, the same below), ④ UB < ZXOT, ⑤ UC < ZXOT. If any of above conditions has occurred, it judges the three-phase four-wire voltage phase sequence is error. Criterion of Three-phase three-wire: ① YUCBUAB is out of 300°±10°, ② UAB < ZXOT, ③ UCB < ZXOT. If any of above conditions has occurred, it judges the three-phase three-wire voltage phase sequence is error.	RO	0
2	LostVoltSC	= 0, the high 16-bit of the total Voltage RMS UC≥ the threshold of LostVoltage (0x04) , phase C is not loss of voltage. = 1, the high 16-bit of the total Voltage RMS UC＜the threshold of LostVoltage (0x04) , phase C is loss of voltage.	RO	0
1	LostVoltSB	= 0, the high 16-bit of the total Voltage RMS UB≥ the threshold of LostVoltage (0x04) ,phase B is not loss of voltage. = 1, the high 16-bit of the total Voltage RMS UB ＜the threshold of LostVoltage (0x04) ,phase B is loss of voltage.	RO	0
0	LostVoltSA	= 0, the high 16-bit of the total Voltage RMS UA≥ the threshold of LostVoltage (0x04), phase A is not loss of voltage. = 1, the high 16-bit of the total Voltage RMS UA＜the threshold of LostVoltage (0x04) ,phase A is loss of voltage.	RO	0

3.4.32.Checksum Register

3.4.32.1.CHECKSUM1 Register (0x6A)

Address: 6AH; Word length: 3bytes

Bit(s)	Name	Description	R/W	Reset
23:0	CHECKSUM1	CHECKSUM1 is the checksum register of the metering module configuration register, and the checksum calculation address range is BANK1 EMM calibration register and EMM configuration register 00H~5AH, 5DH~62H, 64H, 90H, 95H~96H, B0H-BBH. The checksum algorithm negates the sum of three bytes, and if the register length is less than three bytes, it is completed by zero. Note: 1. When D2FCFG[3:0]=4'b1001, B0H~BBH does not participate in the CHECKSUM1 checksum. When D2FCFG[3:0]≠4'b1001, B0H~BBH participates in the CHECKSUM1 checksum with 3 bytes. 2. When DMA_WAVECON2 [17:11] the corresponding bit matches 1, 0x1A~0x20 does not participate in the CHECKSUM1 checksum. 3. When WREN2 writes before the expansion, 0CH~12H, 37H~39H participate in the CHECKSUM1 checksum. After writing the expansion, 0CH~12H, 37H~39H participate in the CHECKSUM3 checksum.	RO	0x3A215C

3.4.32.2.CHECKSUM2 Register (0x8B)

Address: 8BH; Word length: 2 bytes.

Bit(s)	Name	Description	R/W	Reset
15:0	CHECKSUM2	The CHECKSUM2 register is the checksum of NVM1, NVM2, and the system configuration register, which calculates the address range including BANK1 NVM1, NVM2, and system configuration registers 70H, 72H-75H, 83H-86H. The checksum algorithm negates the sum of two bytes, and if the register length is less than two bytes, it is completed with zero.	RO	0xE9DB

3.4.32.3.CHECKSUM3 Register (0xAE)

Address: AEH; Word length: 4 bytes.

This register is the checksum of the chip partial configuration register, and the algorithm is the same as the previous two checksum registers, which is 4 bytes accumulated and negated.

Bit(s)	Name	Description	R/W	Reset
31:0	CheckSum3	CHECKSUM3 REGISTER IS THE CHECKSUM OF THE NEWLY ADDED CONFIGURATION REGISTER, AND THE CHECKSUM CALCULATION ADDRESS RANGE INCLUDES 5BH, 5CH, 6BH, 6DH, 93H, 97H~9DH, A2H~ADH, CBH~DFH, E7H~EDH. The	RO	0xFFFC07FB

		checksum algorithm negates the sum of four bytes, and if the register length is less than four bytes, it is completed by zero. Note: 1. DMA_WAVECON. [13:4] represents the real-time automatic WAVECNT value, which is not counted in CHECKSUM3, and this register bit is processed with 0 and read out as the real-time WAVECNT value; When this register bit is a manually configured value, it participates in the CHECKSUM3 calculation and reads out as the configured value. 2. When WREN2 writes the expansion, 0CH~12H, 37H~39H participate in the CHECKSUM1 checksum. After writing the expansion, 0CH~12H, 37H~39H participate in the CHECKSUM3 checksum.		

3.4.32.4. CHECKSUM4 Register (0xEF)

Address: EFH; Word length: 4 bytes.

This register is the checksum of the key configuration register of the chip, and the algorithm is the same as the previous three checksum registers, which is 4 bytes accumulated and negated.

Bit(s)	Name	Description	R/W	Reset
31:0	CheckSum4	The CHECKSUM4 register is the checksum of the newly added key configuration register, which includes the following key registers (indicated in parentheses: bank field, address, number of bytes, default): (B1 A0H 2 0x40) (B1 9FH 4 0x457) (B1 F4H 4 0xFFFF) (B1 F5H 4 0xFFFF) (B1 F6H 4 0x41) (B1 F7H 4 0xC00) (B1 F8H 4 0x500) (B1 F9H 4 0x07BB_BBBB) (B1 FCH 4 0x455AA) The checksum algorithm negates the sum of four bytes, and if the register length is less than four bytes, it is completed by zero. (The above address F4 to FC This register reserves internal parameter configuration registers for the chip, note that it cannot be modified)	RO	0xF83DD8C4

3.4.33.No-voltage Register NVM1

3.4.33.1.NVM1CFG Register (0x70)

Address: 70H; Word length: 1 byte; Default: 0x01.

NVM1CFG register is used to configure the interrupt enable in the NVM1 mode.

Bit(s)	Name	Description	R/W	Reset
7:4	Reserved	Reserved	RO	--
3	NVM1CMPIE	The no-voltage calculation completes the comparison interrupt enable. =1, enabled. =0, not allowed. No-voltage is calculated and at least one I channel exceeds the set threshold to produce an interrupt. This interrupt is only valid in NVM1 mode and not in other modes.	RW	0
2	NVM1UDIE	No-voltage calculation RMS fixed frequency update (25Hz) interrupt enable;	RW	0
1	HPFOFF	NVM1 no-voltage RMS measurement high-pass filter enable. =0: high-pass filter open; =1: high-pass filter off; In EMM mode (including ADCIN mode), it is recommended not to use this bit to turn off high-pass filter, and you can use DMA_WAVECON2.bit6~bit0 to turn off high-pass filter.	RW	0
0	NVM1IE	NVM1 no-voltage RMS measurement interrupt enable. =1, enabled. =0, not allowed. Enabled by default. This interrupt is only valid in NVM1 mode and not in other modes.	RW	1

Note: When HPFOFF=0, that is, when the high-pass filter is turned on, the no-voltage RMS measurement settling time is 1.6s; When HPFOFF=1, that is, when the high-pass filter is off, the settling time of the no-voltage RMS measurement is 80ms, and the user needs to use the dc OFFSET automatic calibration function to calculate the DC OFFSET calibration register of the three currents to replace the high-pass filtering to eliminate the offset error. See sections 3.4.9 and 3.4.42 for details.

3.4.33.2.NVM1IF Register (0x71)

Address: 71H; Word length: 1 byte

NVM1IF register is NVM1 mode status bits.

Bit(s)	Name	Description	R/W	Reset
7:6	Reserved	Reserved	RO	0
5	NVM1CMPCDone	NVM1 mode IC channel measurement ends and is greater than the threshold (IC overflow), which clears after reading	RC	0
4	NVM1CMPBDone	NVM1 mode IB channel measurement ends and is greater than the threshold (IB overflow), which clears after reading	RC	0
3	NVM1CMPADone	NVM1 mode IA channel measurement ends and is greater than the threshold (IA overflow), which clears after	RC	0

Bit(s)	Name	Description	R/W	Default
		reading		
2	NVM1CMPDone	NVM1 no-voltage comparison interrupt flag. The chip receives and responds to the GONVM1 command in other modes, the mode switch is successful, and then the no-voltage calculation is started, and the calculation result is compared with the threshold, and if at least one I channel exceeds the set threshold, the position 1. This bit clears after reading. If NVM1IE=1, position 1 will generate an interrupt, and INTN1 will flip from high to low; This bit clears 0 at the same time as the interrupt, and INTN1 returns to high.	RC	0
1	NVM1UDIF	No-voltage calculation RMS fixed frequency update (25Hz) interrupt flag;	RC	0
0	NVM1Done	NVM1 interrupt flag bit. The chip receives and responds to GONVM1 commands in other modes, and the mode switch is successful; The position 1. The bit is read and cleared. If NVM1IE=1, the interrupt will occur at position 1, and the INTN will flip from high to low. This bit clears to zero and interrupts, and the INT returns to high. The default for this bit power-on reset is 0.	RC	0

3.4.33.3. NVM1 DC OFFSET Calibration Register (0xCB~0xCD)

Address	CBH	CCH	CDH
Register	LS_DCOS_IA	LS_DCOS_IB	LS_DCOS_IC
Default	0x0	0x0	0x0

Bit(s)	Name	Description	R/W
15:0	LS_DCOS	When measuring no-voltage, the DC OFF calibration register, the 2-byte signed number, the OFFSET register shifts 6 bits to the left and the 24-bit sample value is directly added. Effect of LS_DCOS_Ix on RMS_LA1: Taking the IA channel as an example, the relationship between the DC LS_DCOS_IA and the RMS of the no-voltage measurement in RMS_LA1 the IA path can be deduced as follows: $RMS\_LA1' = sqrt((RMS\_LA1^2 + ((LS\_DCOS\_IA - IAd0) * 2^7) / 2^{23})^2)$ LS_DCOS_IA refers to the DCOS register of IA channel under NVM1, which can be any value between 0~0xffff; IAd0 refers to the DCOS_IA register after the DCOS automatically	RW

corrects the completion of the IA channel when the IA channel is unloaded and the ADC input is shorted to ground;

RMS_LA1 refers to the normalized value of any RMS that does not exceed the total scale waveform of the actual input of the IA channel under NVM1;

RMS_LA1' refers to the normalized value of the RMS register actually read out by the IA channel under NVM1;

3.4.33.4. NVM1 Measurement Threshold Configuration Register (0xCE~0xD0)

Address	CEH	CFH	D0H
Register	LS_THOA	LS_THOB	LS_THOC
Default	0x0	0x0	0x0

Bit(s)	Name	Description	R/W	Reset
23:22	LS_TH	This register bit exists only LS_THOA, LS_THOB, LS_THOC register this bit is read-only, defined as follows: =2'b00 NVM1 calculation time is 80ms; =2'b01 NVM1 calculation time is 120ms; =2'b10 NVM1 calculation time is 160ms; =2'b11 NVM1 calculation time is 200ms;	RW	0x0
21:0	LS_Ox	Using phase A as an example, compare the LS_THOA 22 bits lower [21:0] with the lower 22 bits [21:0] of the no-voltage measurement rm RMS_LA1 s of the IA path [21:0] and exceed the threshold when RMS_LA1 [21:0] $\geq$ LS_THOA [21:0] or RMS_LA1 [22]=1. LS_THOA threshold configuration formula: $$LS\_THOA = K* IA*0.87909/ (16* (1+GSIA))$$ IA: Enter the RMS of the rated current in A- phase GSIA: Channel gain of A-phase. K: Total lost-voltage current threshold factor such as 5% Channel gain should be considered when using This configuration is suitable for A/B/C phase	RW	0x0

3.4.34. No-voltage Register NVM2

3.4.34.1. NVM2CFG Register (0x72)

Address: 72H; Word length: 2 bytes; Default: 0x0F21.

NVM2CFG register is used to configure the NVM2 mode.

Bit(s)	Name	Description	R/W	Reset
15:14	Reserved	Reserved	RO	0
13	Lvlsel_cmp[2]	This bit together with [5:4] of the NVM2CFG register controls the comparator, =1, and the comparator threshold is 0.7mV=0, as defined in NVM2CFG[5:4].	RW	0
12:8	NVM2NUM [4:0]	Comparison cycles configuration of the NVM2 current comparison unit. Cycles = NVM2NUM[4:0]+1, Default 5'b01111, indicates the comparison cycles are 16 cycles.	RW	0xF
7:6	Reserved	Reserved.	RW	0
5:4	NVM2TH[1:0]	NVM2 Comparator Level Setting. 	Code	Description
---	---
2'b00	Reserved
2'b01	Comparator level 1, 50mV typical application of current sample Ib
2'b1x (default)	Comparator level 2, 100mV typical application of current sample Ib		RW	0x2
3	Reserved	Reserved.	RO	0
2	FreqSEL	50, 60Hz frequency selection. =0,50Hz; =1, 60Hz. The default is 0.	RW	0
1	Reserved	Reserved	RW	0
0	NVM2IE	NVM2 no-voltage judgment interrupt enable. = 1, enable. = 0, disable, 1 default. Valid in the NVM2 mode only.	RW	1

3.4.34.2.NVM2CMP Register (0x73~0x75)

Address	73H	74H	75H
Register	NVM2CMPA	NVM2CMPB	NVM2CMPC
Default	0x0256	0x0256	0x0256

Bit(s)	Name	Description	R/W	Reset

15:11	Reserved	Reserved	RO	--
10:0	NVM2CMPx	The NVM2 comparator control registers include three NVM2CMP A/B/C REGISTERS for NVM2 triple comparator output processing. The default is 0x0256, note that configuring only NVM2CMPA is equivalent to configuring both NVM2CMPB and NVM2CMPC, and configuring NVM2CMPB or NVM2CMPC does not affect the other two comparator control registers. This register must be initialized to 0x0000 when using NVM2 comparison prediction normally.	RW	0x0256

3.4.34.3. NVM2IF Register (0x76)

Address: 76H; Word length: 1 byte

NVM2 mode status flag register. Valid in the NVM2 mode only.

Bit(s)	Name	Description	R/W	Reset
7	CMPC	NVM2 phase C current comparison result. = 1, phase C current is greater than the level configured in NVM2TH[1:0] within the cycles configured in NVM2TNUM[4:0]. = 0, phase C current is less than the level configured in NVM2TH[1:0] for at least one time within the cycles configured in NVM2TNUM[4:0]. This bit and CMPB,CMPA,CMP are updated when NVM2DONE is set to 1.	RC	0
6	CMPB	NVM2 phase B current comparison result. = 1, phase B current is greater than the level configured in NVM2TH[1:0] within the cycles configured in NVM2TNUM[4:0]. = 0, phase B current is less than the level configured in NVM2TH[1:0] for at least one time within the cycles configured in NVM2TNUM[4:0].	RC	0
5	CMPA	NVM2 phase A current comparison result. = 1, phase A current is greater than the level configured in NVM2TH[1:0] within the cycles configured in NVM2TNUM[4:0]. = 0, phase A current is less than the level configured in NVM2TH[1:0] for at least one time within the cycles configured in NVM2TNUM[4:0].	RC	0
4	CMP	NVM2 polyphase current comparison result. = 1, three phase currents are greater than the level configured in] within the cycles configured in NVM2TNUM[4:0]. = 0, at least one of three phase currents is less than the level configured in NVM2TH[1:0] for at least one time within the	RC	0

		cycles configured in NVM2TNUM[4:0].		
3:1	Reserved	Reserved	RO	0
0	NVM2Done	NVM2 current comparison end flag. Be set to 1 after start up and complete the NVM2 comparison for one time. Meantime, CMP/CMPA/CMPB/CMPC are updated. Cleared once the following situation has occurred, ① Cleared after the read, ② Cleared when switch to other modes (SLM/NVM1/EM) from NVM2 or switch to NVM2 from other modes. =1 will cause INT interrupt when NVM2IE = 1 in NVM2CFG,. When this bit is cleared ,the interrupt is cleared, and INTN is set back high.	RC	0

3.4.35.Write Enable Register

3.4.35.1.WREN Register (0x80)

Address: 80H, Word length: 1 byte, Default: 0x00.

This register is used for partially readable write-protect commands for write-safe registers. After power-on reset and software reset, the register returns to the default write-protected state. The protection address is: 00H~5AH, 5FH~65H, 70H~75H, 77H, 81H~89H, 90H~92H, 94H, 9EH~A1H, B0H~BBH, F0H~F1H, F3H~FAH.

Command	Command Word	Description
WREN	0xE5	Write enable command. After the write enable is valid, all R/W registers are Write Enabled. This register is read as 0x01.
WRDIS	0xDC	The write protection command. After the write protection is valid, all R/W registers are write protection. This register is read as 0x00.
	Others	Reserved.

3.4.35.2.WREN2 Register (0x7F)

Address: 7FH; Word length: 4 bytes; Default:0x00.

This register is used for partially readable write-safe registers and partial register expansion commands. After power-on reset and software reset, the register returns to the default write-protected state. Protection address: bank1: 5DH~5EH, 6BH~6DH, 78H, 93H, 95H~9DH, A2H~ADH, C8H~E3H, E5H~E7H, FCH, FEH; bank0:D0H~D2H, D4H~F6H, F8H.

Bit(s)	Command	Command Word	Description
3116	Reserved		Reserved

15:8	WREN2	0xE5	Write the enable command. When write enable is active, some of the MKE304T readable and writable registers are write enabled, and the register bits are read as 0x01.
	WRDIS2	0xDC	Write protect commands. When write protection is active, some MKE304T readable write-protected registers, which are read as 0x00.
7:0	EXTEN_EN	0xAA	Expand command. After the command is valid, all the expansion registers (Bank1 0CH~12H, 37H~39H, 8DH) need to be expanded, and the register bits are read as 0x01. Note: 1.After the Px_OS register is enabled by the expansion command, it needs to be configured EMUCFG3.P_OS_SEL=1, and the upper 16 bits take effect; Otherwise 16 bits high is writable but does not work. 2.PHSxx register needs to configure PHSUA[31:24]=0xA7 after the expansion command is enabled, and the value of other phase calibration registers after expansion is cleared to zero, to make the phase calibration register configuration value after expansion work, it is necessary to ensure that PHSUA[31:24]=0xA7 when writing the configuration value; Otherwise, the write is invalid. 3.The Wdata register holds the last SPI write value for 3 bytes before WREN2 write is enabled; After WREN2 write enable, save the last SPI write value for 4 bytes and add a 4-byte configuration register for save. The number of bytes is insufficient to make up for the high bit.
	EXTEN_DIS	0x55	Expand restore command. After the command is valid, all required expansion registers (Bank1 0CH~12H, 37H~39H, 8DH) are restored to the original word length, and the register bits are read as 0x00.

3.4.36.Operating Mode Switching Register

3.4.36.1.WSWM Mode Status Register (0x81)

Address: 81H; Word length: 1 byte

This register is used to configure the operating mode. The initial value of this register after the power-up reset reflects the default operating mode after the reset determined by the pin PM. PM = 1, the initial value is 0x03. PM = 0, the initial value is 0x01.After the mode switching, this register is the current operating mode flag.

Command	Command Word	Description
GOSLM	0x18	If the system is in EMM/NVM1/NVM2 mode and register is write enable, receiving and responding to this command will switch to SLM. After the mode switching is completed, this register = 2'b11. Meantime, WMS[1:0] = 2'b11 in SYSSR (0x8A).

Command	Command Word	Description
		Receiving this command in SLM mode,not activated.
GONVM2	0x5C	If the system is in SLM/EMM/NVM1 mode and register is write enable, receiving and responding to this command will switch to NVM2 and complete the criterion of the NVM2 current comparison for one time. After the mode switching is completed, this register = 2'b10. Meantime, WMS[1:0] = 2'b10 in SYSSR (0x8A). After the criterion of the current comparison is completed, NVM2DONE=1 in the NVM2IF register. Receiving this command in NVM2 mode,not activated.
GONVM1	0xE1	If the system is in SLM/NVM2 mode and register is write enable, receiving and responding to this command will cause to generate the wake-up reset, then switch to NVM1 mode and start NVM1 current RMS calculation after the reset. If the system is in EMM mode, receiving and responding to this command will switch to NVM1 mode, and start NVM1 current RMS calculation. After the mode switching is completed, this register = 2'b00. Meantime, WMS[1:0] = 2'b00 in SYSSR (0x8A). NVM1Done in the NVM1IF register is set to 1 after 450ms. Receiving this command in NVM1 mode,not activated.
GOEMM	0xA2	If the system is in SLM/NVM2 mode and register is write enable, receiving and responding to this command will cause to generate the wake-up reset, and then switch to EMM mode and start all functions in EMM mode after the reset. If the system is in NVM1 mode, receiving and responding to this command will switch to EMM mode, and start all functions in EMM mode. After the mode switching is completed, this register = 2'b01. Meantime, WMS[1:0] = 2'b01 in SYSSR (0x8A). Receiving this command in EMM mode, not activated.
--	Others	Reserved.

3.4.36.2.ADCIN Mode Configuration Register ADCIN_WREN (0xA1)

Address: A1H; Word length: 1byte.

Command	Command Word	Description
	0xEA	Enable ADCIN_CFG registers; The register reads as 0x2.
	0x00	Turn off enable, write protection; The register reads as 0.
	Otehrs	Invalid

3.4.36.3.ADCIN Mode Configuration Register ADCIN_CFG (0xA0)

Address: A0H; Word length: 2bytes; Default: 0x0040.

The chip supports each sampling channel to configure whether it is internal or external, when bit12 bits are selected as 1, bit3~bit5 and bit7 configurations are invalid; When bit12 is configured as 0, bit3~bit5 and bit7 support separate configuration ADC internal or external.

Bit(s)	Name	Description	R/W	Reset
15:14	Reserved	Reserved	RO	0
13	CKO_SEL	The default is 0, only in ADCIN mode, and ADCIN_WREN write enabled, this register is writable. =0: The ADIN_CKO pin (including the CF multiplexing pin) outputs a 4.096MHz clock; =1: The ADIN_CKO pin (including the CF multiplexing pin) outputs a 2.048MHz clock.	RW	0
12	ADCIN_UADC_SEL	The default is 0, which is writable only in ADCIN mode and ADCIN_WREN write enabled. =1 U channel 1bit source from internal ADC; =0 U channel 1bit source from BIT3~BIT5.	RW	0
11:8	ADCIN_SOFT_EN	ADCIN mode software enable. =4'hA, only in EMM mode, the chip will switch from EMM to ADCIN mode; Read as 1. =4'h5, only in ADCIN mode, the chip will exit ADCIN mode and switch to EMM mode; Read as 0. = Other value, invalid configuration. It is recommended that chips with mode configuration pins use mode configuration pins to enter ADCIN mode	RW	0
7	ADCIN_PUT	=0, the IN-channel ADC in ADCIN mode is external; =1, IN-channel ADC internal in ADCIN mode;	RW	0
6	Reserved	Reserved, the default is 1, keep the R/W property	RW	1
5	ADCUC_PUT	When ADCIN_UADC_SEL=0, =0, UC channel ADC in ADCIN mode is external; =1, UC channel ADC internal in ADCIN mode; When ADCIN_UADC_SEL=1, the bit configuration is invalid.	RW	0
4	ADCUB_PUT	When ADCIN_UADC_SEL=0, =0, the UB channel ADC in ADCIN mode is external; =1, the UB channel ADC in ADCIN mode is internal; When ADCIN_UADC_SEL=1, the bit configuration is invalid.	RW	0
3	ADCUA_PUT	When ADCIN_UADC_SEL=0, =0, the UA channel ADC in ADCIN mode is external;	RW	0

		=1, UA channel ADC internal in ADCIN mode; When ADCIN_UADC_SEL=1, the bit configuration is invalid.		
2	ADCIC_PUT	=0, the IC channel ADC in ADCIN mode is external; =1, IC channel ADC internal in ADCIN mode;	RW	0
1	ADCIB_PUT	=0, the IB channel ADC in ADCIN mode is external; =1, IB channel ADC internal in ADCIN mode;	RW	0
0	ADCIA_PUT	=0, the IA channel ADC in ADCIN mode is external; =1, IA channel ADC internal in ADCIN mode;	RW	0

In ADCIN mode, there are two polyphase shunt meter application schemes, scheme 1: four-channel current channel ADC external, three-channel voltage channel ADC internal; Solution 2: All seven ADCs are external. There are multiple package types on the chip, and software configuration is required for the missing configuration to enter the ADCIN mode pin, and the two package types are configured to enter the ADCIN mode of the two schemes as shown in the following table:

Packaging type	Solution 1: Four-channel current channel ADC external, three-channel voltage channel ADC internal;	Solution 2: All seven ADCs are external
Pins with mode (ADIN_MOD, PM) Software + Pins	Pins: 1. ADIN_MOD=1; 2. PM=0; Software: 3.Bank1 0x80H write 0xE5; 4.Bank1 0xA1H write 0xEA; 5.Bank1 0xA0H write 0x1040; Software Reliability: 6.Read Bank1 0xA0H as 0x1040.	Pins: 1.ADIN_MOD=1; 2.PM=0; Software: 3.Bank1 0x80H write 0xE5; 4.Bank1 0xA1H write 0xEA 5.Bank1 0xA0H write 0x0040 Software Reliability: 6.Read Bank1 0xA0H as 0x0040
Pins without mode Software only	Software: 1.Bank1 0x80H write 0xE5; 2.Bank1 0xA1H write 0xEA 3.Bank1 0xA0H write 0x1A40 Software Reliability: 4.Read Bank1 0xA0H as 0x1A40	Software: 1.Bank1 0x80H write 0xE5; 2.Bank1 0xA1H write 0xEA 3.Bank1 0xA0H write 0x0A40 Software Reliability: 4.Read Bank1 0xA0H as 0x0A40

Note: When the chip enters ADCIN mode, the WSWM mode status register reads 0x5 indicating that the current operating mode is normally external ADC metering mode.

3.4.37.Software Reset Register SOFTRST (0x82)

Address: 82H, Word Length: 1 byte, Default: 0x00.

Command	Command Word	Description
SOFTRST	0xFA	Software reset command. When register write is enabled, writing this command will cause the software to reset. This register is a WO attribute.
	0x69	Software reset EMU (including EMU, NVM) calculation module: In the write-enabled state, write 0x69 reset EMU computing module; This register is a WO attribute.
	0xB4	Software reset EMU (including EMU, NVM) registers: In the write-enabled state, write 0xB4 reset EMU configuration register; This register is a WO attribute.
	0xD2	FLK module register and calculation module software reset: In the write enabled state, write 0xD2 reset the flicker module; This register is a WO attribute.
	0xE1	In the write-enabled state, the MMU waveform buffer DMA state machine software resets 0xE1 write and the register is a WO attribute.
	0x87	In the write-enabled state, write 0x87 and the SPI state machine is soft reset, which is a WO attribute.
	0x4C	In the write-enabled state, the write 0x4C and the HSDC state machine is reset, and this register is a WO attribute.
	0xA5	In the write-enabled state, write 0xA5, ECT software reset, the module configures registers and state machine resets, which are WO attributes.
	others	Invalid. The chip does not operate.

3.4.38. ADC Configuration Register ADCCFG (0x83)

Address: 83H, Length: 2 bytes, Default: 0x0000.

The ADCCFG register is used to configure seven ADCs.

Bit(s)	Name	Description	R/W	Reset
15	PGAIN_16	IN channel analog gain 16 times select: =0, according to the PGAIN[1:0] configuration to determine the IN_PGA. =1, the analog gain of the IN channel is 16x, and the PGAIN[1:0] configuration is invalid.	RW	0
14	REFSEL	The ADC reference voltage selection. = 0, select on-chip reference voltage as reference voltage of ADC. = 1, select external REF as reference voltage of ADC. 0, by default.	RW	0

13:12	PGAIN[1:0]	PGA gain for IN.	RW	0
11:10	PGAIC[1:0]	PGA gain for IC.	RW	0
9:8	PGAIB[1:0]	PGA gain for IB.	RW	0
7:6	PGAIA[1:0]	PGA gain for IA.	RW	0
5:4	PGAUC1:0]	PGA gain for UC.	RW	0
3:2	PGAUB[1:0]	PGA gain for UB.	RW	0
1:0	PGAUA1:0]	PGA gain for UB.. = 2'b00, 1X. = 2'b01, 2X. = 2'b10, 4X. = 2'b11, 8X. 2'b00 by default.	RW	0

3.4.39.Error Wiring Measurement Calibration Register

3.4.39.1.TTEEC_EN-- Three-phase three-wire error wiring measurement calibration enable register (0x5E)

Address: 5EH; Word length: 1 byte; Default: 0x0. After reset, the register returns to its default state (three-phase three-wire incorrect wiring metering calibration function is turned off).

Command	Command Word	Description
TTEEC_EN	0x51	Three-phase three-wire error wiring measurement calibration enabled. After the three-phase three-wire error wiring measurement calibration is enabled: 1) This register is 0x01 2) FGPA,FGPB,FGPC,FGQA,FGQB,FGQC,FPA_PHS,FPB_PHS,FPC_PHS,FQA_PHS,FQB_PHS,FQC_PHS register range changes to ±2。 3) The fundamental channel power gain calibration and power phase calibration change the calculation of fundamental power parameters, and the formula is: fundamental active $FP2=FP1*FGP*2+FQ1*FPphs*2$; Fundamental reactive power $FQ2=FQ1*FGQ*2-FP1*FQphs*2$. (except RMS Fundamental Apparent) 4) The influence of total channel power gain calibration and power phase calibration on total power parameters remains unchanged to ±1, and the calculation formula remains unchanged. 5) RMS apparent and RMS fundamental apparent are only relevant for apparent power gain calibration and the calibration formula does not change.
	0x00 (default)	The three-phase three-wire error wiring measurement calibration function

		is turned off. FGPA,FGPB,FGPC,FGQA,FGQB,FGQC,FPA_PHS,FPB_PHS,FPC_PHS ,FQA_PHS,FQB_PHS,FQC_PHS register range recovery.
	others	Invalid, the chip does not operate.

3.4.39.2.TFEEC_EN-- Polyphase, four-wire error wiring measurement calibration enable register (0x84)

Address: 84H; Word length: 1 byte; Default: 0x00. After reset, the register returns to its default state.

Command	Command Word	Description
TFEEC_EN	0x42.	Three-phase four-wire incorrect wiring measurement calibration enabled. After the write command word is 0x42 and valid: 1) The register reads as 0x01 2) UCHSEL and ICHSEL registers are writable
	0x00 (default)	The three-phase four-wire error wiring metering calibration function is turned off. 1) This register reads as zero 2) UCHSEL and ICHSEL registers are not writable.
	others	Invalid, the chip does not operate.

3.4.39.3.ICHSEL—current channel selection register (0x85)

Address: 85H; Word length: 1 byte; Default: 0x00.

The current channel selection register configures the path from the I1/I2/I3 output of the sampling channel to the EMU IA/IB/IC channel.

Bit(s)	Name	Description		R/W	Reset
7:6	Reserved	Reserved		RO	0
5:0	ICHSEL[5:0]	I1 control;		RW	0
		Ichsel[1:0]=00 I1; =01 I1; =10 I2; =11 U3;			
		I2 control;		RW	0
		Ichsel[3:2]=00 I2; =01 I1; =10 I2; =11 I3;			
		I3 control;		RW	0
		Ichsel[5:4]=00 I3; =01 I1; =10 I2; =11 I3;			

This register is valid when three-wire four-phase error wiring calibration (TFEEC_EN) is enabled, and if the three-wire four-phase error wiring calibration is turned off, the register is not writable and reads zero.

Note: (1) NVM1 no-voltage judgment, ICHSEL [5:0] to participate in the no-voltage judgment mark NVA, N VB and NVC logic judgment, IA, IB and IC no-voltage judgment mark NVA, NVB and NVC to correspond to the current channel determined by ICHSEL [5:0].

3.4.39.4.UCHSEL—voltage channel selection register (0x5D)

Address: 5DH; Word length: 1 byte; Default: 0x0

The voltage channel selection register configures the path from the sampling channel U1/U2/U3 output to the EMU UA/UB/UC channel。

Bit(s)	Name	Description		R/W	Reset
7:6	Reserved	Reserved		RO	0
5:0	UCHSEL[5:0]	U1 control;		RW	0
		Uchsel[1:0]=00 U1; =01 U1; =10 U2; =11 U3;			
		U2 control;		RW	0
		Uchsel[3:2]=00 U2; =01 U1; =10 U2; =11 U3;			
		U3 control;		RW	0
		Uchsel[5:4]=00 U3; =01 U1; =10 U2; =11 U3;			

This register is valid when three-wire four-phase error wiring calibration (TFEEC_EN) is enabled, and if the three-wire four-phase error wiring calibration is turned off, the register is not writable and reads zero.

3.4.40.Three-phase four-wire/Three-phase three-wire Mode Selection Register MODSEL (0x86)

Address: 86H, Length: 1 byte, Default: 0x00.

The MODSEL register is used to select the three-phase four-wire and three-phase three-wire mode.

Bit(s)	Name	Description
MODSEL	0x33	Three-phase three-wire mode enable. Select three-phase three-wire. After it is valid, read as 0x01.
	0x00(default)	Three-phase four-wire mode enable. Default. Select three-phase four-wire. After it is valid, read as 0x00.
	other	Reserved.

3.4.41.System Configuration Register SYSCFG (0x78)

Address: 78H; Word length: 4 bytes; Default: 0x38A00.

SYSCFG provides clock gating for each module, power switch, and separate power switch for each channel measurement ADC.

Bit(s)	Name	Description	R/W	Reset
31:24	SYS_PS	Write the password bits, password is 0xEA. = 0xEA, the lower 17 bits are writable; = Other values, lower 17 bits are not writable.	WO	0
23:19	Reserved	Reserved	RO	0
18	INTN2_OUT_EN	INTN2 interrupts the output pin state configuration, 0: the pin state is high-impedance state 1: the pin state is output state	RW	0
17:16	Reserved	Reserved	RO	0
15	Reserved	Reserved, keep at 1	RW	1
14	NVM2_CK_EN	NVM2 clock gating: Valid only for EMM mode configuration, default is 0, other mode configuration is invalid. =0: Clock stopped, module cleared =1: Clock started, module enabled	RW	0
13	ECT_CK_EN	Error temperature compensation module enabled to zero, clock gating: only active in EMM mode configuration, other mode clock off =0: The clock stops and clears the module =1: Clock starts, module enables	RW	0
12	HSDC_CK_EN	HSDC module enabled to clear, clock gating: only active in EMM mode configuration, other modes clock off = 0: clock stop, module zero = 1: clock start, module enable	RW	0
11	NVM1_CK_EN	NVM1 module enabled to clear, clock gating: only the configuration is valid in EMM mode, the default is 1, other modes are off, the configuration is invalid. 0: Clock stop, module clear; 1: Clock start, module enable.	RW	0
10	FLK_CK_EN	Flicker module enabled to clear, clock gating; Only the configuration is valid in EMM mode, the default is 0, other modes are off, the configuration is invalid. 0: Clock stop, module clear;	RW	0

		1: Clock start, module enable.		
9	ADC_CK_EN	Pass-induced ADC clock output enabled to zero, clock gating: configured in EMM/ADCIN/NVM1 mode and turned off in all other modes. Note: In EMM mode, you need to configure ADCIN_CFG.bit11~bit9=0xA, and the clock output can only be ADIN_CKO pin.	RW	1
		0: clock stop;		
		1: clock strat.		
8:7	Reserved	Reserved	RO	0
6	ADCIN_PD	IN-channel ADC power switch. This bit is configured in EMM mode NVM1 mode, and in SLM/NVM2 mode, the ADC is forced to power down and the configuration is invalid.	RW	0
		0: power on		
		1: power down		
5	ADCUC_PD	UC channel ADC power switch. This bit is only valid in EMM mode configuration, where the ADC is forced to power down and the configuration is invalid in SLM/NVM1/NVM2 mode.	RW	0
		0: power on		
		1: power down		
4	ADCUB_PD	UB channel ADC power switch. This bit is only valid in EMM mode configuration, where the ADC is forced to power down and the configuration is invalid in SLM/NVM1/NVM2 mode.	RW	0
		0: power on		
		1: power down		
3	ADCUA_PD	UA channel ADC power switch. This bit is only valid in EMM mode configuration, where the ADC is forced to power down and the configuration is invalid in SLM/NVM1/NVM2 mode.	RW	0
		0: power on		
		1: power down		
2	ADCIC_PD	IC channel ADC power switch. This bit is configured in	RW	0

		EMM mode/NVM1 mode, and in SLM/NVM2 mode, the ADC is forced to power down and the configuration is invalid.		
		0: power on		
		1: power down		
1	ADCIB_PD	IB channel ADC power switch. This bit is configured in EMM mode/NVM1 mode, and in SLM/NVM2 mode, the ADC is forced to power down and the configuration is invalid.	RW	0
		0: power on		
		1: power down		
0	ADCIA_PD	IA channel ADC power switch. This bit is configured in EMM mode/NVM1 mode, and in SLM/NVM2 mode, the ADC is forced to power down and the configuration is invalid.	RW	0
		0: power on		
		1: power down		

Note: In metering mode, SYSCFG.ADCxx_PD the configuration is turned off, the digital and analog parts of the ADC will be turned off at the same time, at which time the subsequent metering functions of the channel are all turned off, and the resulting register is read out as a fixed value;

3.4.42. System Status Register SYSSR (0x8A)

Address: 8AH, Length: 2 bytes

The SYSSR register is used to reflect the operating status of the chip.

Bit(s)	Name	Description	R/W	Reset
15:14	WMS[1:0]	The operating mode status bit. | WMS[1:0]	Description | |---|---|
2'b 11	Current operating mode is SLM.
2'b 10	Current operating mode is NVM2.
2'b 01	Current operating mode is EMM.
2'b 00	Current operating mode is NVM1.		RO	--
13	PM	PM pin status bit. = 1, the PM pin inputs is high. = 0, the PM pin inputs is low.	RO	--

12	Reserved	It is always 1.	RO	--
11	MODSEL	The three-phase three-wire/three-phase four-wire mode status bit. = 1, the system is in the three-phase three-wire mode. = 0, the system is in the three-phase four-wire mode.	RO	--
10	Reserved	Reserved.	RO	--
9	Reserved	Reserved.	RO	--
8	Reserved	Reserved.	RO	--
7	REG_WE	Write Enable flag. =1, the configuration register is write enable. =0. the configuration register is write protection.	RO	--
6	Reserved	Reserved.	RO	--
5	REF_OK	Reserved.	RO	--
4	Reserved	Wake-up reset flag. =1,the NVM2 or SLM mode is switched to EMM or NVM1, or the power-up reset default mode is EMM or NVM1. During the reset, this bit is 0. Cleared after read.	RO	--
3	WKR_FLAG	Reserved.	RC	--
2	SRST_FLAG	Software reset flag. During the software reset, =0. When the software reset is completed, =1. Cleared after read, and cleared after the power-up and power-down reset.	RC	--
1	RSTN_FLAG	External pin reset flag. When the external pin reset is complete, =1. Cleared after read, and Cleared after the power-up and power-down reset.	RC	--
0	PWROK_FLAG	3.3V power supply monitoring reset flag. When the 3.3V power-up and power-down is completed, =0. Cleared after read.	RC	--

3.4.43.SPI Check Register

3.4.43.1.WData Register (0x8D)

Address: 8DH; Word length: 3 or 4 bytes.

Bit(s)	Name	Description	R/W	Reset
23(31):0	WData	The WData register holds the data written by the previous SPI and can be used for verification when the SPI writes the data. When the register word length of the previous secondary SPI is less than three bytes, the lower bytes are aligned. Note: This register is the default three-byte until the WREN2 expand command is enabled; After the expand command, the register becomes 4 bytes to read the previous SPI write data, the word length is less than four bytes, and the low bytes are aligned.	RO	0

3.4.43.2.Waveform buffer address register (0x8E)

Address: 8EH; Word length: 2 bytes.

Bit(s)	Name	Description	R/W	Reset
15:0	LRBufAddr	The LRBufAddr register represents the address of the last waveform buffer data when SPI burst reads waveform buffer data. For example, when a burst mode read waveform buffer ends, the register points to the address of the last read data buffer. In Burst mode read, when the last read data address crosses the bounds, that is, > 4FFH, the LRBufAddr register does not do special processing and still saves the out-of-bounds address.	RO	---

3.4.44.DeviceID Register

3.4.44.1.DeviceID register (0x8F)

Address: 8FH, Length: 3 bytes

Bit(s)	Name	Description	R/W	Reset
15:0	DeviceID	The DeviceID register represents the DeviceID number of the chip, which is always 830200H after power on.	RO	0x830200

3.4.44.2.DeviceID2 register (0xFF)

Address: FFH; Word length: 3bytes.

Bit(s)	Name	Description	R/W	Reset
23:0	DeviceID2	The DeviceID2 register represents the DeviceID number of MKE304T , which is always 830201H after power on.	RO	0x830201

3.4.45. Voltage angle and frequency measurement threshold registers ZXOTU (0x90)

Address: 90H; Word length: 2 bytes.

Bit(s)	Name	Description	R/W	Reset
15:0	ZXOTU	The current angle calculation threshold will only use ZXOT (0x05). ZXOT (0x05) is used by default for voltage angle calculation and frequency measurement threshold, ZXOTU (0x90H) can be selected as the voltage zero crossing and frequency measurement threshold when ZXOTCFG [4]=1 (0x92H), and ZXOT is selected as the voltage zero crossing and frequency measurement threshold when ZXOTCFG [4]=0. When the RMS of a channel is less than the value of the zero-crossing threshold register, the channel does not output zero crossing, and the phase angle of the channel is not calculated, and the phase angle of the channel outputs 0x000000. Frequency measurement thresholds are described in the Voltage Line Frequency Registers section. The zero-crossing threshold register ZXOTU(0x90) is a 2-byte unsigned number, which is compared with the RMS Ux (x=A, B, C) bit27-bit12 bits of each phase voltage for judgment. The initial Reset of the ZXOTU is 0x0000, which can be reset by the user as needed. This register participates in the calculation of checksum register 1 (0x6AH). The ZXOTU calculation formula is the same as the zero-crossing threshold register in Section 3.4.1.2.	RW	0x0

3.4.46. Zero-crossing Calculate Configuration and Flag Register ZXOTCFG (0x92)

Address: 92H; Word length: 2 bytes. This register does not participate in checksum calculations.

Bit(s)	Name	Description	R/W	Reset
16:12	Reserved	Reserved	RO	0
11:5	ZXFLAG	Read-only bit, which stores the angle calculation flag bit of each channel, and 1 indicates that the channel participates in the angle calculation; 0 means not participating, the angle register is read out as 0, and the order is {IN/IC/IB/IA/UC/UB/UA}	RO	0x0
4	ZXOTUS	=1, the voltage angle and frequency measurement calculation threshold are selected as ZXOTU; =0, the voltage angle and frequency measurement calculation threshold are selected as ZXOT.	RW	0x0
3	ZXOTUBS	=1, the voltage of B channel participates in the angle calculation when the three-phase three-wire is three-wire; =0, the B-way voltage does not participate in the angle calculation when the three-phase three-wire is three-wire;	RW	0x0

2	ZXOTUC	=1, the UC channel participates in the angle calculation; =0, select whether UC participates in angle calculation based on the threshold comparison result.	RW	0x0
1	ZXOTUB	=1, the UB channel participates in the angle calculation; =0, select whether UB participates in the angle calculation based on the threshold comparison results.	RW	0x0
0	ZXOTUA	=1, the UA channel participates in the angle calculation; =0, select whether UA participates in angle calculation based on the threshold comparison results.	RW	0x0

3.4.47. DC OFFSET Automatic Calibration Register AUTODC_EN (0x91)

Address: 91H; Word length: 2 bytes; Default: 0x0000. This register does not participate in checksum calculations.

AUTODC_EN register is used to initiate the automatic calculation of the 7-way ADC dc OFFSET and reflect the completion status.

Bit(s)	Name	Description	R/W	Reset
15:8	Reserved	Reserved	RO	0
7	EMM_DC_DIS	=0, the DC offset auto-calibration result is that the DCOS register affects the metering channel parameters and NVM1 current RMS calculation. =1, DC offset automatic calibration result, that is, the DCOS register only affects NVM1 current RMS calculation, does not affect the metering channel parameter calculation, suitable for NVM1 needs offset calibration and metering path does not need the occasion.	RW	0
6	IN_DC_EN	Simultaneous sampling 6-channel mode: At IN_WaveEN(B1 0x94)=1, the simultaneous sampling IA channel is occupied by IN traffic. To complete the DC offset calibration of IN, write 1 to in this bit to start the IN automatic offset calibration, and after the calibration is completed, the bit is cleared, and the DC offset value of the IN channel is DCOS_IN obtained, and the DC offset value of the IN channel is also obtained DCOS_IA. Synchronous sampling 7-channel mode: When IN_WaveEN(B1 0x94)=0, IN and IA data streams flow independently in their respective synchronous sampling channels, the bit writes 1 to start IN automatic offset calibration, and after the calibration is completed, the bit is cleared to zero, and the DC offset value of the IN channel is DCOS_IN obtained.	RW	0
5	UC_DC_EN	Write 1 to start UC automatic offset calibration, at which point the input should be grounded or no-load; After 128 cycles, the calibration is automatically completed, the bit is automatically	RW	0

		cleared after the calibration is completed, and the calibration result is written to the DCOS_UC register.		
4	IC_DC_EN	Write 1 to starts IC automatic offset calibration, at which point the input should be grounded or no-load; After 128 cycles, the calibration is automatically completed, the bit is automatically cleared after the calibration is completed, and the calibration result is written to the DCOS_IC register.	RW	0
3	UB_DC_EN	Write 1 to start UB automatic offset calibration, at this time the input should be empty; After 128 cycles, the calibration is automatically completed, the bit is automatically cleared after the calibration is completed, and the calibration result is written to the DCOS_UB register.	RW	0
2	IB_DC_EN	Write 1 to start IB automatic offset calibration, at which point the input should be grounded or no-loaded; After 128 cycles, the calibration is completed automatically, the bit is automatically cleared after the calibration is completed, and the calibration result is written to the DCOS_IB register.	RW	0
1	UA_DC_EN	Write 1 to start UA automatic offset calibration, at this time the input should be unloaded; After 128 cycles, the calibration is automatically completed, the bit is automatically cleared after the calibration is completed, and the calibration result is written to the DCOS_UA register.	RW	0
0	IA_DC_EN	Write 1 to start IA automatic offset calibration, at which point the input should be grounded or no-load; After 128 cycles, the calibration is automatically completed, the bit is automatically cleared after the calibration is completed, and the calibration result is written to the DCOS_IA register.	RW	0

Note: When EMM_DC_DIS=0, that is, the DCOS register affects the metering channel parameters; If you are using DC offset calibration only in NVM1 mode, you should let EMM_DC_DIS=1.

Note: The DC offset calibration register (1AH~20H) is involved in the checksum calculation.

EMM mode and NVM1 mode use the same current DC offset calibration register:

1DH	1EH	1FH
DCOS_IA	DCOS_IB	DCOS_IC

When EMM_DC_DIS=1, the DCOS register only affects NVM1 current RMS calculation, and automatic calibration is initiated by IA_DC_EN, IB_DC_EN, and IC_DC_EN, and the register needs to be divided by 0.512 for current channel DC offset calibration under NVM1。

Simultaneous sampling 6-channel mode:

DCOS_IN. IN_DC_EN only meaningful when IN_WaveEN (94H) = 1, the DC offset value of the IN channel can be obtained, and the IA channel data in the waveform buffer data is all replaced with the IN channel. If IN_WaveEN=0, then the value obtained by DCOS_IN is actually the IA channel value. That is, if you want to get the DC offset bias of 7 channels, you need to do it in two steps, the first step to get the value of 6 channels, and the second step to get the value of the IN channel。

Synchronous sampling 7-channel mode:

When IN_WaveEN (bank1 94H)=0, IN and IA data streams flow independently in their respective synchrono us sampling channels, the bit writes 1 to start the IN automatic offset calibration, and after the calibration is compl eted, the bit is cleared to zero, and the DC offset value of the IN channel is DCOS_IN obtained.

3.4.48.Waveform Buffer Enable Register IN_WaveEN (0x94)

Address: 94H; Word length: 2 bytes; Default: 0x0000. This register does not participate in checksum calculations.

IN_WaveEN register is used to enable IN waveform buffer.

Bit(s)	Name	Description	R/W	Reset
15:1	Reserved	Reserved	RO	0
0	IN_WaveEN	=1 Select the IN channel waveform buffer instead of the IA channel waveform buffer; Select the IN channel DC offset automatic calibration to replace the IA channel; =0 Disables IN channel waveform buffer and IN DC offset auto-calibration functions.	RW	0

3.4.49.Half-cycle Update Active Power Calculation Point Configuration Register HW_PNum (0xE8)

Address: E8H; Word length: 4 bytes; Default: 0x00000000

This register is WREN2 write protected, the default is 0, representing the active power of the half-cycle updat e is calculated according to the half-cycle 80-point accumulation average, the minimum support is based on the ha lf-cycle 1-point accumulation average calculation, the maximum support half-cycle 511-point half power accumul ation averaging calculation, defined as follows:

Bit(s)	Name	Description	R/W	Reset
31:9	Reserved	Reserved	RO	0
8:0	PNum	The active power accumulation for half-cycle update is averaged: = 9'b0, and the average calculation is calculated by the accumulation of 80 points of the half-cycle; = 9'b1, calculated by averaging the accumulation of 1 point in the half-period; = 9'b1x, calculated as the half-period 2-point accumulation average; = 9'b1xx, calculated by averaging the accumulation of 4 points in the half-period; = 9'b1xxx, calculated by averaging the accumulation of 8 points in the half-period; = 9'b1xxxx, calculated by averaging the accumulation of 16 points in the half-period; = 9'b1xxxxx, calculated as the half-period 32 points accumulated to find the average; = 0x40~0x1FF, if the expected half-cycle accumulation is N, then PNum = N, and the software determines the number of half-cycle sampling points N.	RW	9'b0

3.4.50. Half-cycle Update Reactive Power Calculation Point Configuration Register HW_QNum (0xE9)

Address: E9H; Word length: 4 bytes; Default: 0x00000000

This register is WREN2 write protected, the default is 0, representing the half-cycle update of the reactive po wer according to the half-cycle 80-point accumulation average, the minimum support for half-cycle wave 1-point accumulation average calculation, up to support half-cycle 511 points half power accumulation average calculatio n, defined as follows:

Bit(s)	Name	Description	R/W	Reset
31:9	Reserved	Reserved	RO	0
8:0	QNum	The reactive power for half-cycle update is calculated by accumulation and averaging: = 9'b0, calculated by the accumulation of 80 points of the half-cycle wave; = 9'b1, calculated by averaging the accumulation of 1 point in the half-period; = 9'b1x, calculated as the half-period 2-point accumulation average; = 9'b1xx, calculated by averaging the accumulation of 4 points in the half-period; = 9'b1xxx, calculated by averaging the accumulation of 8 points in the half-period; = 9'b1xxxx, calculated by averaging the accumulation of 16 points in the half-period; = 9'b1xxxxxx, calculated as the half-period 32 points accumulated to find the average; = 0x040~0x1FF, if the expected half-cycle accumulation to find the average number of points is N, then QNum = N, and the software determines the number of half-cycle sampling points N.	RW	9'b0

3.4.51. Half-cycle Update Power Update Mode Configuration Register HW_MODCFG (0xEA)

Address: EAH; Word length: 4 bytes; Default: 0x0.

This register is WREN2 write-protected and is used to select the mode for half-cycle update power registers.

Bit(s)	Name	Description	R/W	Reset
31:4	Reserved	Reserved	RO	0
3	FQ_ZoN_SEL	=0, the fundamental reactive power updated half-cycle is calculated by selecting a fixed number of points, and the number of points is configured by the HW_QNum (B1 0xE9); =1, the fundamental reactive power updated half-	RW	0

		cycle is calculated by choosing the method of zero-crossing.			
2	FP_ZoN_SEL	=0, the fundamental active power of half-cycle update is calculated by selecting a fixed number of points, and the number of points is configured by HW_PNum (B1 0xE8); =1, the fundamental active power of half-cycle update is calculated by choosing the method of zero-crossing.	RW	0
1	Q_ZoN_SEL	=0, the total reactive power updated half-cycle is calculated by selecting a fixed number of points, and the number of points is configured by HW_QNum (B1 0xE9); =1, the total reactive power updated half-cycle is calculated by zero-crossing.	RW	0
0	P_ZoN_SEL	=0, the total active power updated half-cycle is calculated by selecting a fixed number of points, and the number of points is configured by HW_PNum (B1 0xE8); =1, the total active power of half-cycle update is calculated by choosing the method of zero-crossing;	RW	0

3.5. Effect of Reset and Mode Switching on Registers

3.5.1. Power-on and Power-down Reset

PM Pin	ADIN_MOD	Mode after reset	Register
0	0	EMM	1. All registers reset. 2. After reset, start the EMM function; NVM1 and NVM2 features are turned off.
0	1	ADCIN	1. All registers reset. 2. After reset, start the ADC metering function; NVM1 and NVM2 features are turned off.
1	0	SLM	1. NVM1 configuration and status register, NVM2 configuration and status register, system configuration and status register reset. 2. The parameter register, EMM calibration register, EMM configuration, and status register are invalid.

3.5.2. Outside Pins Reset

Mode before reset	Mode after reset	Register
EMM	EMM	1. NVM1CFG, NVM1CMPA, NVM1CMPB, NVM1CMPC (hereinafter referred to as NVM1 configuration register) remain unchanged. 2. NVM2 configuration register NVM2CFG remains

		unchanged.
		3. The system configuration registers WREN, WREN2, ADCCFG, MODSEL remain unchanged.
		4. Other registers reset.
NVM1	NVM1	Ditto
NVM2	NVM2	1. NVM1 configuration register, NVM2 configuration register, and system configuration registers WREN, WREN2, ADCCFG, MODSEL remain unchanged. 2. After reset, start the NVM2 current comparison function once to refresh the NVM2IF register. 3. The parameter register, EMM calibration register, EMM configuration, and status register remain invalid. 4. Other registers reset.
ADCIN	ADCIN	1. The system configuration registers WREM, ADCCFG, MODSEL remain unchanged. 2. Other registers reset.

Note: The chip RSTN pin (default pull-up) receives a low signal for ≥ 1ms, and a pin reset occurs

3.5.3.Software Reset

Mode before reset	Mode after reset	Register
EMM	EMM	1. NVM1 configuration register, NVM2 configuration register, system configuration register ADCCFG, MODSEL remain unchanged. 2. Other registers include WREN, WREN2 reset.
NVM1	NVM1	Dittio
NVM2	NVM2	1. NVM1 configuration register, NVM2 configuration register, and system configuration registers ADCCFG and MODSEL remain unchanged. 2. After reset, start the NVM2 current comparison function once to refresh the NVM2IF register. 3. The parameter register, EMM calibration register, EMM configuration, and status register remain invalid. 4. Other registers include WREN, WREN2 reset.
ADCIN	ADCIN	1. The system configuration registers WREM, ADCCFG, MODSEL remain unchanged. 2. Other registers reset.

3.5.4.Mode Switching and Registers

Current mode	Mode switching command	Mode after switching	Register changes
SLM or NVM2	GOEMM	EMM	1. A wake-up reset occurs, and the parameter register, EMM calibration register, EMM configuration, and status register are reset. 2. After reset, start the EMM function; NVM1 single measurement and NVM2 function off. NVM1 25Hz update RMS function is enabled. 3. The SYSSR register, operating mode switching register, and NVM2IF have changed accordingly. 4. The other registers remain unchanged.
	GONVM1	NVM1	1. A wake-up reset occurs, and the parameter register, EMM calibration register, EMM configuration, and status register are reset. 2. After reset, start the NVM1 RMS current measurement function, and refresh the NVM1 RMS current register; The EMM function is invalid, and the EMM parameter register and status register hold the Reset. 3. The SYSSR register, operating mode switching register, and NVM2IF have changed accordingly. 4. The other registers remain unchanged.
EMM 或 NVM1	GOSLM	SLM	1. The parameter register, EMM calibration register, EMM configuration, and status register are invalid. 2. The SYSSR register and the operating mode switching register and NVM1IF register change accordingly. 3. The other registers remain unchanged.
EMM 或 NVM1	GONVM2	NVM2	1. The parameter register, EMM calibration register, EMM configuration, and status register are invalid. 2. Start the NVM2 current comparison function once to refresh the NVM2IF register. 3. The SYSSR register and the operating mode switching register and NVM1IF register change accordingly. 3. The other registers remain unchanged.
EMM	GONVM1	NVM1	1. The EMM calibration register, EMM configuration, and status register are invalid, but retain the values before the switchover. 2. Start the NVM1 RMS current measurement function, and refresh the NVM1 RMS current register. The EMM function is not valid, but the EMM parameter registers hold the value before the switch. 3. SYSSR register and operating mode switching register and NVM1IF register change accordingly 4. Other registers remain unchanged
NVM1	GOEMM	EMM	1. Start the EMM function, the EMM calibration register, EMM configuration register are active, and the EMM parameter register and EMM status register start to refresh.

			2. Turn off the NVM1 RMS Current 1 (single update) measurement function, and the NVM1 RMS 1 register holds the value before switching. NVM1 current RMS 2 (25Hz update) continues to update. 3. The SYSSR register and the operating mode switching register change accordingly. 4. The other registers remain unchanged.
NVM2	GOSLM	SLM	1. The parameter register, EMM calibration register, EMM configuration, and status register are invalid. 2. The SYSSR register and the operating mode switching register and NVM2IF register change accordingly. 3. The other registers remain unchanged.
SLM	GONVM2	NVM2	1. The parameter register, EMM calibration register, EMM configuration, and status register are invalid. 2. Start the NVM2 current comparison function once, and the NVM2IF register is refreshed. 3. The SYSSR register and the operating mode switching register change accordingly. 4. The other registers remain unchanged.

3.6. Register Write Protection

In addition to the write-enable registers, all readable and writable registers and command registers are write-protected.

The readable and writable registers after power-on reset and software reset default state is write-protected. Write enable register 1 turns off write protection after receiving the WREN command. After receiving the WRDIS command, enable write protection. Write enable register 2 turns off write protection after receiving the WREN2 command, and enables write protection after receiving the disturb WRDIS2 command.

The REG_WE status bits in the SYSSR register reflect the write-protected state of the chip's current register.

3.7. Register write expansion

After the WREN2 register receives the EXTEN_EN expand command, all the bits that need to be expanded by the expansion register (Bank1 0CH~12H, 37H~39H, 8DH) are expanded from the default byte length to the new byte length. The extended checksum follows the new rules, see the Checksum Register section; After the expand command is enabled, the function takes effect as described in the WREN2 Register section.

After the WREN2 register receives the EXTEN_DIS expand restore command, the expansion register restores the default byte length, and the register function under the default length takes effect.

4.Calibration

4.1.Introduction

Provide a wealth of calibration methods to realize software calibration, which supports both the power calibration method and the traditional pulse calibration method. Corrected instrumentation with both active and reactive accuracy of 0.2S. The calibration methods of the chip include:

- The meter constant is adjustable via the HFConst register

- ADC sampling channel gain calibration

- ADC sampling channel phase calibration, where three current channels support segmented phase calibration

- Active, reactive and apparent power gain calibration

- Active and reactive power phase calibration, support segmented phase calibration

- Offset calibration of active, reactive power, and RMS

- It has the function of automatic verification of calibration meter data

4.2.Power Mode Calibration
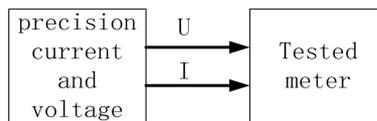
Compared with the traditional pulse calibration method, the power method calibration has the advantages of simple and fast calibration. Its calibration system is shown in the figure, only one high-precision current and voltage source is required, and the accuracy level of the source should be higher than the level required by the meter under test.

4.2.1.Calibration Process

Fig.4-1 calibration process

Power mode calibration process:

1. Calculate the standard U and I registers when the rated input is calculated, and calculate the standard active power values when calculating PF=1.0 and PF=0.5L; And the HFConst of the chip is calculated according to the meter constant.

2. Set up the calibration environment according to the figure and set the parameters, such as configuring the ADC PGA gain, HFConst, threshold register, etc. of the chip.

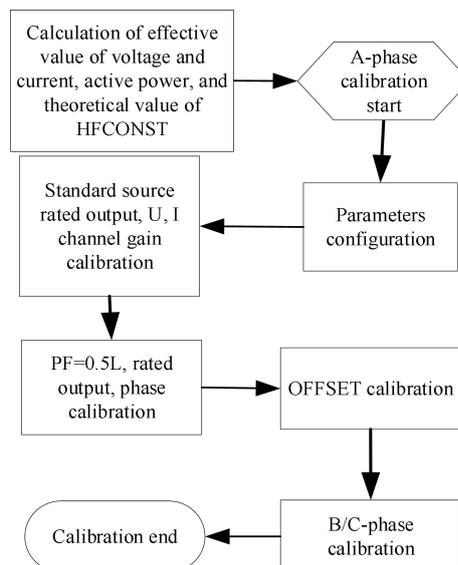3. The standard source rated output, read the actual voltage and current RMS of phase A, and calculate the error with the theoretical value, and then calculate the value of the voltage and current channel gain register of phase A according to this error, fill in and compare the calibration results, and complete the gain calibration of the U and I channels of phase A.

4. Standard source PF=0.5L, rated output, read out the active power of phase A and calculate the error with the theoretical value, and then calculate the value of the channel phase register or power phase register according to this error, fill in and compare the calibration results, and complete the phase calibration of the A phase channel.

5. Standard source current no-load, read the no-load RMS and power value, and then calculate the corresponding OFFSET value according to the no-load value and fill in the value of the corresponding OFFSET register. Complete the A-phase OFFSET calibration (this option is optional).

6. The same method completes the gain, phase, and OFFSET calibration of other phases.

7. End of the calibration schedule.

4.2.2. Standard voltage, current and active power values calculation

1. Calculate and select standard voltage RMS registers

For voltage rated inputs, the standard voltage RMS register should be both convenient for the MCU to convert to the LCD display value and within a reasonable range of channel gain calibration.

Assuming that the voltage rating input Un, the voltage RMS at the input of the chip voltage channel is Vu, and the theoretical calculation value is $U_{theoretical}$, LCD display value is converted by the MCU to $U_{display}$, the standard RMS voltage register is $U_{standard}$, so $U_{standard}$ should select to meet the following conditions:

$0.8 < U_{standard}/U_{theoretical} < 1.2$

$K = U_{standard}/U_{display}$, K should be an integer and easy for MCU conversion.

The first condition above ensures that the U-channel gain correction is within a reasonable range, and the second condition, K, should be selected to facilitate the MCU to convert the RMS register to the LCD display value. If PGA=1, $U_{theoretical}$ can be calculated as follows

$U_{theoretical} = INT[(Vu/830)*2^{27}]$

2. Calculate and select standard current RMS registers

The same principle is used to calculate the standard RMS current register for the current rated input $I_{standard}$

3. Calculate PF=1.0 and PF=0.5L, standard active power registers

Rated input, PF=1.0, standard active power value $P = INT(U_{standard} * I_{stadard}/2^{23})$

Rated input, PF=0.5L, standard active power value $P_{0.5L} = INT(U_{standard} * I_{standard}/2^{24})$

4.2.3. HFConst calculate

According to PF=1.0, the standard active power value P, meter constant EC and other parameters calculate the theoretical HFConst value as follows:

$HFConst = INT[P*3.6*10^6*fosc / (32*EC*Un*Ib*2^{31})]$

P: PF=1.0, calculated by 3) the standard active power register

Fosc: Crystal frequency, it is recommended to connect an external 8.192Mhz crystal

Un: Rated input voltage;

Ib: Rated input current;

EC: Meter constant

Configure the HFConst1 and HFConst2 registers as calculated.

4.2.4.Parameters configuration

The parameter setting process is shown in Figure 4-2:
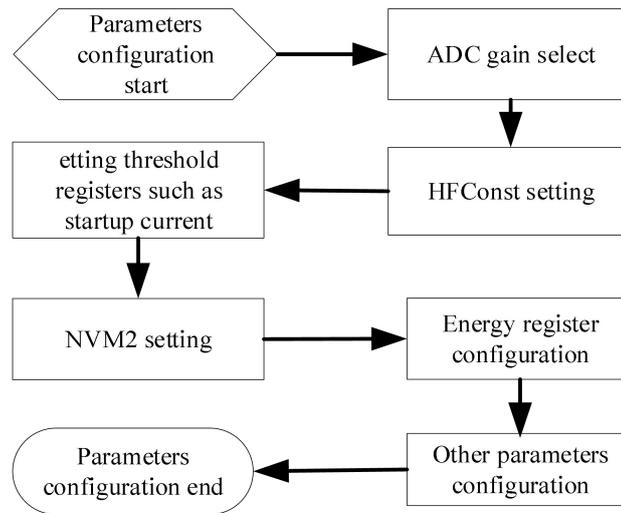
Figure 4-2 Parameters Configuration

1. ADC gain selection, configure ADCCFG registers.

2. HFCosnt settings, populating the theoretical HFConst values calculated in Section 4.2.3 into the HFConst1 and HFConst2 (optional) registers.

3. Threshold registers include start-up current threshold, phase compensation area threshold, loss of voltage threshold, zero crossing threshold, voltage sag threshold, overvoltage overcurrent threshold register. The threshold is calculated according to the standard voltage and current RMS calculated in section 4.2.2, and the corresponding threshold register is filled in, as described in the 3.4 Configuration and Status Registers section.

4. NVM2 setting, according to the Ib point input, select the appropriate NVM2 gear, select the NVM2 cycle wavenumber, and configure the NVM2CFG register.

5. Energy register settings, configure the accumulation mode of the energy register, three-phase four-wire/three-phase three-wire selection, zero-clearing type and accumulation type selection, etc., the method is detailed in the 3.2.6 energy register chapter.

4.2.5.Channel gain calibration

Standard source rated output, assuming that if Section 4.2.2 calculates the standard RMS voltage of phase A as UA, the standard RMS current is IA, the readout phase A RMS register is UA', and the RMS real current register is IA', then:

A-phase voltage RMS error $ErrUA= (UA'-UA)\ /UA$

A-phase current RMS error $ErrIA= (IA'-IA)\ /IA$

A-phase U-channel gain correction can be achieved by configuring the GSUA register, which is calculated as follows:

$$USGain = \frac{-ErrUA}{1+ErrUA}$$

If USGain>=0, then $GSUA=INT[USGain*2^{15}]$

Or USGain<0, then $GSUA=INT[2^{16}+USGain*2^{15}]$

Phase A I channel power gain correction can be achieved by configuring the GSIA registers in the same way as GSUA.

Through this method, the correction error of the RMS of the rated output can be controlled at 0.02%~0.03%. After the correction of the RMS of phase A voltage and the RMS current, the gain of active power/reactive power/apparent power/fundamental correlation and power is all corrected. Since HFconst is derived from the ideal value of power, the energy error under phase resistance A is also automatically corrected.

4.2.6.Phase calibration

The standard source configuration is changed to PF=0.5L, that is, the power factor angle is 60°, and the rated output, assuming that if Section 4.2.2 calculates that the ideal active power of phase A is $PA_{0\ 5L}$, and the actual active power readout is $PA_{0\ 5L'}$, then the active power error of phase A caused by phase error is:

$$ErrPA= (PA_{0.5L}'-PA_{0.5L})\ /PA_{0.5L}$$

This error can be corrected by the channel phase correction method, that is, by configuring the phase correction register PHSUA of the A phase U channel or PHSIA of the phase correction register of the I channel. Phase compensation formula: if the angular difference between the U and I channels of A-phase is θ, then

$$\theta = \mathrm{Arcsin}\ \frac{-ErrPA}{\sqrt{3}}$$

If θ >0, indicates that UA is ahead of IA; If θ <0, indicates UA lag IA. For 50HZ, PHSUA and PHSIA registers have a relationship of 0.017578°/LSB, that is, when adjusting 1 LSB and the power factor angle is 60°, the active error changes by 0.053% and the reactive error changes by 0.02%.

If you adjust the PHSUA register, there is $PHSUA = 0x80+INT(\theta/0.017578°)$

If the PHSIA register is adjusted without considering segment correction, there is:

$PHSIA\_R1[7:0] = 0x80-INT(\theta/0.017578°)$

When the WREN2 register is enabled, the channel phase correction register is extended to 4 bytes, and when the upper 8 bits of PHSUA [31:24] of PHSUA[31:0] (0x30) are written to the 0xA7, the meaning of all channel phase correction registers changes, as defined below, see section 3.4.7 Channel Phase Correction Registers. With PHSUA [31:24] already written to 0xA7, all channel phase correction registers were changed from 8bit to 10bit. The calibration scale was increased from 0.017578°/LSB to 0.008789°/LSB, and the calibration range was extended from ±2.25 o or 4.5° to ±4.5°or 9°.

The correction formula is the same as the default situation above, and only 0.017578 needs to be modified to 0.008789 to achieve a correction range of ± 4.5°. If you want to achieve a correction range of 9°, you only need to write the register of the PHSU to 0, and then change the PHSI (from 0x000 to 0x3ff); Or write the register of PHSI to 0 and change the PHSU (from 0x000 to 0x3ff).
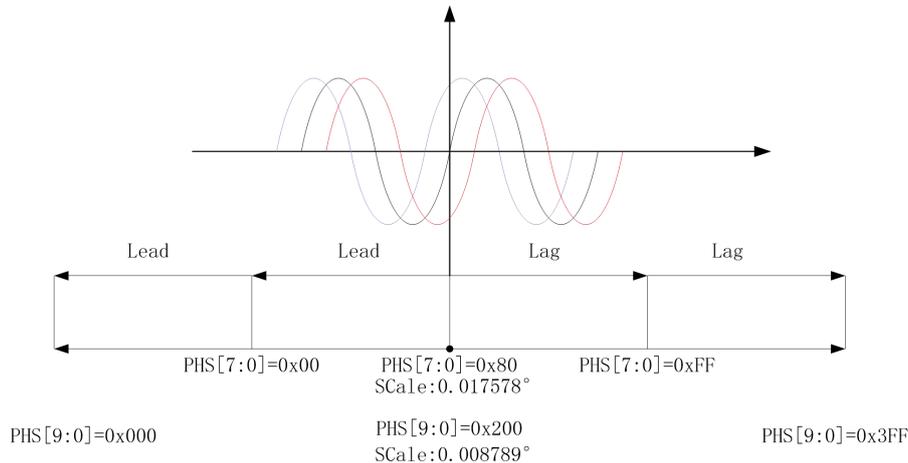
When the user needs to control the active phase error of PF=0.5L within ±0.03%, it needs to be corrected by the power phase correction method, if the segmentation correction is not considered, the user can configure the A phase active power phase correction register PA_PHSL and the A phase reactive power phase correction register QA_PHSL to achieve correction. Phase compensation formula:

$$\lambda = \frac{-ErrPA}{\sqrt{3}}$$

If $\lambda \geq 0$, then *PA_PHSL*= λ *2^{15}; If $\lambda <0$, then *PA_PHSL*= λ *$2^{15}+2^{16}$

If $\lambda \geq 0$, then *QA_PHSL*= λ *2^{15}; If $\lambda <0$, then *QA_PHSL*= λ *$2^{15}+2^{16}$

This method has high requirements for the phase accuracy and stability of the standard source.

4.2.7. RMS OFFSET Calibration

OFFSET correction is an effective means to improve the accuracy of small signals when external noise (PCB noise, transformer noise, etc.) is large, which affects the accuracy of small signals (such as 1%Ib). If external noise has little effect on the accuracy of the small signal, this step can be ignored.

Current OFFSET calibration description:

Taking the RMS of A phase current as an example, the register calculation process IA_OS:

1) Configure the standard source so that U=Un, the current channel input is no-load;

2) The MCU reads the RMS current register, and averages 10 data continuously IAavereg (read once in 250ms);

3) Find the square of IAave2; In general, this value will not exceed 2^29-1, if it exceeds 2^29-1 after the square, then it is beyond the range that the offset register can correct, and will not play the purpose of OFFSET correction, but will become larger and larger;

4) Take the bit14~bit29 of the IAave2 negative number (- IAave2) complement (shift 14 bits to the right and take the lower 16 bits), and fill in the IA_OS register.

5) Current RMS offset calibration end.

The same process is the same for the RMS current OFFSET and fundamental current RMS for the other phases.

Formula:

IX_OS =-Ix_avreg²/ 2¹⁴

Where: Ix_avreg is (IA/IB/IC) the average of some current register.

Example: With a current input of zero, the value of the read RMS current register is 0x0000483, and (the average can be read several times) the decimal number is 1155.

After squaring it, find its inverse code: 1155*1155=1334025=0x145B09, and the 32-bit complement is 0Xffeba4f7.

Take bit29~bit14 (0Xffeba4f6 divided by 2^14) to obtain 0x FFAE write current RMS bias correction register.

4.3.Power Mode Calibration Example

Suppose you design a sample table with a 220v(Un), 1.5A(In) rated input and a table constant of 1000(EC). The rated voltage Un=220V, the signal amplitude of the corresponding ADC input is required to be Vu=220mv; Rated current Ib=1.5A; The signal amplitude of the corresponding ADC input is Vi=50mV, and the analog channel gain is 1 times.

1. Standard voltage RMS register calculation and selection

   1) Calculate the theoretical value of the RMS voltage register at the rated input

According formula $U_{theoretical}=INT[(Vu/830)*2^{27}]$, bring Vu=220mV in, yield:

$U_{theoretical}$= INT[(220/830)*2^{27}]=35575783

   2) According condition: $0.8 < U_{standard}/U_{theoretical} < 1.2$, $U_{standard}$ reasonable selection range is 28640626~42690940

3) The LCD display value is converted by the MCU to $U_{display}$=220V, the selectable $U_{standard}$ is 42,000,000, and the MCU can be easily converted.

2. Standard current RMS register calculation and selection

1) Calculate the theoretical value of the RMS current register at the rated input

According formula $I_{theoretical}=INT[(Vi/830)*2^{27}]$, bring Vu=50mV in, yield:

$I_{theoretical}$= INT[(50/830)*2^{27}]=8085405

2) According condition $0.8 < I_{standard}/I_{theoretical} < 1.2$, $I_{standard}$ reasonable selection range is 6468324~9702486

3) The LCD display value is converted by the MCU to $I_{display}$=1.5A, $I_{standard}$ can select as 7500000, that MCU can convert conveniently.

3. PF=1.0 and PF=0.5L, standard active power register calculate.

Rated input, PF=1.0, standard active power value:

$P = INT(U_{standard}* I_{standard}/2^{23})$=42000000*7500000/$2^{23}$=37550926

Rated input, PF=0.5L, standard active power value

$P_{0.5L}= INT(U_{standard}* I_{standard}/2^{24})$= 37550926/2=18775463

4. HFConst calculation and configuration

According formula: $HFConst = INT[P*3.6*10^6*fosc / (32*EC*Un*Ib*2^{31})]$

$= INT[(37550926*3.6*8.192*10^{12})/ (32*1000*220*1.5*2^{31})]$

$= 48833 = BEC1H$

So that the chip configure HFConst1= HFConst2=BEC1H.

5. Parameters configuration

Omitted.

6. Channel gain calibration process

Standard source rated output, readout A-phase RMS register, assuming 37297350, then

$ErrUA= (UA'-UA) /UA=(37297350-44000000)/44000000=-0.152333,$

Write $[-ErrUA/(1+ErrUA)*2^{15}]=[0.1797085*32768]=5888=1700H$ into register GSUA, so that the voltage RMS register can calibrate as 44000000, The calibration error can be controlled in 0.02%~0.03%.

Read out the phase A current RMS register, assuming 8299685, then

$ErrIA= (IA'-IA) /IA=(8299685-7500000)/7500000= 0.106625, -ErrIA/(1+ErrIA)= -0.0963515,$

Write $INT[65536-0.0963515*32768]=F3ABH$ into register GSIA; In this way, the RMS current can be corrected to 7500000, and the correction error can be controlled in 0.02%～0.03%.

After the correction of the RMS of phase A voltage and the RMS of current, the active power/reactive power/fundamental related RMS and power are all corrected. Since HFconst is BEC1H derived from standard active power, the A-phase energy error is also automatically corrected.

Phases B and C are corrected according to the same process.

7. Phase calibration process

After calibrating the channel gain, change the power factor to 0.5L, and read out the active power register of phase A as 19526535, then

$ErrPA= (PA_{0.5L}'-PA_{0.5L}) /PA_{0.5L} = (19526535-19669533) /19669533=-0.00727$

If channel phase correction is used, then θ=ArcSin (- (-0.00727) /1.732) =ArcSin0.0042=0.2406° 。PHSUA=128+INT[0.2406/0.017578]=142, converting to decimal 16 is 0x8E

If power phase correction is used, then λ =- (-0.00727) /1.732=0.0042; PA_PHSL= λ *2^{15}=138, converting to decimal 16 is 0x89; QA_PHSL= λ *2^{15}=138, converting to decimal 16 is 0x89.

Phases B and C are corrected according to the same process.

4.4.Pulse Mode calibration
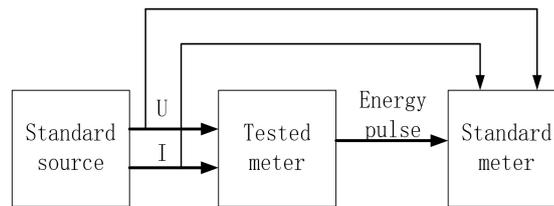
When the user has a stable but average accuracy level standard source, but has a higher level of standard table, the pulse calibration method as shown in the figure above can be considered. The calibration process of the pulse mode calibration is shown in Figure 4-3
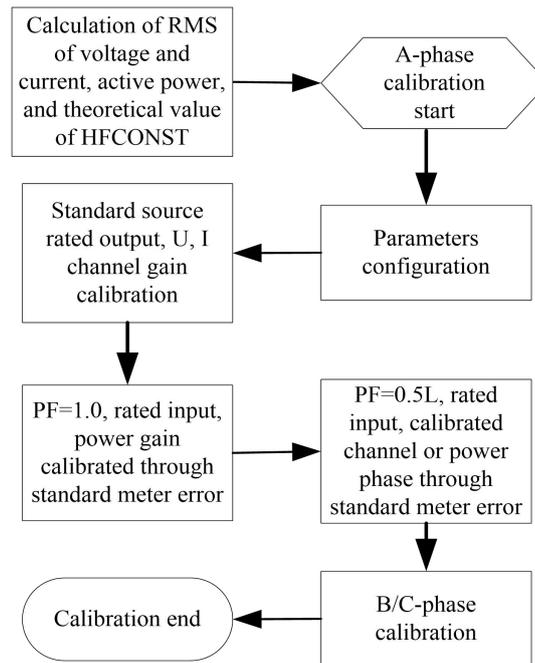
Figure 4-3 Pulse mode calibration

The first few steps of the pulse calibration process and the power method calibration process are the same, except that the standard meter error is used to calculate the power gain register and phase registers during gain correction and phase calibration.

The method of estimating the value of the power gain register from the standard table PF=1.0 is detailed in Section 3.4.11. After GPA is adjusted, GQA, GSA, FGPA, FGQA, FGSA can fill in the same values. The method of estimating the channel phase register from the standard table PF=0.5L error is detailed in Section 3.4.7. The method of estimating the power phase register from the standard table PF=0.5L error is detailed in Section 3.4.12.

5.Communication Interface

- Supports serial communication interface SPI. Work in a subordinate mode.

- SPI interface rate: 3.5Mbps maximum

- Transmission reliability: The SPI frame format contains checksum bytes

- The read buffer supports Burst 4/8/16/32/64 modes

- 3.3V/5V compatible

5.1.SPI Address Space Description

Address AD[10:0] mapping:

0x000~0x0FF : Measurement parameter register space, belonging to BANK0 (abbreviated as B0)

0x100~0x1FF : Configuration and status register space, belonging to BANK1 (abbreviated as B1)

0x200~0x27F : Waveform sampling data buffer block 1 space, belonging to BANK2 (abbreviated as B2)

0x280~0x2FF : Waveform sampling data buffer block 2 space, belonging to BANK2 (abbreviated as B2)

0x300~0x37F : Waveform sampling data buffer block 3 space, belonging to BANK3 (abbreviated as B3)

0x380~0x3FF : Waveform sampling data buffer block 4 space, belonging to BANK3 (abbreviated as B3)

0x400~0x47F : Waveform sampling data buffer block 5 space, belonging to BANK4 (abbreviated as B4)

0x480~0x4FF : Waveform sampling data buffer block 6 space, belonging to BANK4 (abbreviated as B4)

0x500~0x57F : Waveform sampling data buffer block 7 space, belonging to BANK5 (abbreviated as B5)

0x600~0x611 : Measurement register 2 space, belonging to BANK6 (abbreviated as B6)

5.2.SPI Interface Signal Description

SCSN: SPI selects signal from the device chip, active low, input signal, internal floating, it is recommended to connect an external pull-up resistor.

When the SCSN changes from high to low, it means that the current chip is selected and in the communication state; When the SCSN changes from low to high, it means that the communication is over and the communication port reset is idle.

SCLK: The serial clock input pin determines the transfer rate at which data is moved out of or into the SPI port.

All data transfer operations are synchronized with the SCLK, and the chip outputs data from the SDO pin on the SCLK rising edge; The host outputs data from the SDI pin on the SCLK rising edge. Both the chip and the host read data on the SCLK falling edge.

SDI: Serial data input pin. It is used to transfer host data to the inside of the chip.

SDO: Serial data output pin, used to output chip data to the host. When the SCSN is high, it is a high-impedance state.

5.3.SPI Frame Format

SPI frames include read register frames, write register frames, and BURST read waveform data buffer frames. The transmission process for each frame is as follows:

Write operation:

SPI Master Drive	ADDR	CMD	MSB	⋯	LSB	CS

Read operation:

SPI Master Drive | ADDR | CMD

SPI Slave Drive | MSB | ··· | LSB | CS

Where:

ADDR bytes: Contains AD[7:0], which refers to the lower octet address of the destination address

CMD bytes: contains {R/W, AD[10:8], BL[1:0], BL[2], 1'b0}, where

R/W=0, indicating a read operation; R/W=1, indicating a write operation;

AD[10:8] , which indicates the upper 3 bits of the destination address, that is, the Bank address;

BL[2:0] , which indicates the word length of the Burst read operation (that is, how many addresses of data are read);

BL[2:0]=3'b000, read a register or a waveform, not burst read;

BL[2:0]=3'b001, Burst reads 4 words in length, and reads 4 registers or waveform data of consecutive addresses

BL[2:0]=3'b010, Burst reads 8 words in length, and reads 8 registers or waveform data of consecutive addresses

BL[2:0]=3'b011, Burst reads 16 words long and reads 16 registers or waveform data for consecutive addresses

BL[2:0]=3'b100, Burst read word length is 32, only waveform data reading is available, read 32 waveform data of consecutive addresses

BL[2:0]=3'b101, Burst read word length is 64, only waveform data reading is available, read 64 waveform data of consecutive addresses

When R/W=0 and BL[2:0] is not 0, and the address falls in the waveform sampling data buffer space, the waveform data burst reading is performed. When the waveform data burst is read, the address is "incremented" in the "increment" mode, and when the address "increments" beyond the waveform sampling data buffer space, the read waveform is invalid, but its value still participates in the checksum calculation.

When R/W=0 and BL[2:0] is not 0, the address falls on the register address, that is, a register burst read occurs. When the register burst reads, the register address is also "incremented", when the address "increments" beyond the register address space, that is, more than 1FFH, the address remains unchanged, and the read register is 0.

When writing operations, BL is invalid, but its value still participates in checksum calculation;

MSB, LSB bytes: data blocks; High byte first, low byte second;

CS block: Checksum bytes.

Word length: The waveform data burst read each data fixed length is 24bit, register burst read each register readout length is fixed at 32bit.

These three types of SPI frame formats are described in Table 5-1.

Table 5-1 MKE304T SPI frame formats

Command Name	ADDR	CMD	DATA	CHECKSUM	Description
Read Register	{REG_ADR[7:0] }	{1'b0, BANK[2:0] , 4'b0000} BANK=3'b000, register	RDATA	The frame checksum is calculated	Read data from registers with address

Frame		address maps to metering parameter register address space BANK=3'b001, register address maps to register address space of configuration and status registers.		and emitted by the MKE304T.	{BANK[2:0],REG_ADR[7:0]}.
Write Register Frame	{REG_ADR[7:0]}	{1'b1, BANK[2:0], 4'b0000} BANK=3'b000, register address maps to metering parameter register address space BANK=3'b001, register address maps to register address space of configuration and status register BANK=3'b110, register address maps to metering parameter register 2 address space	WDATA	The write register frame checksum is calculated and issued by the MCU.	Write data to registers with address {BANK[2:0],REG_ADR[7:0]}.
BURST Read Waveform Data Buffer Frame	{BUF_ADR[7:0]}	{0,BANK[2:0], Burst_LEN[2:0], 1'b0} BANK=3'b010-3'b101 ADDRESS maps to waveform buffer RAM address space Burst_LEN[2:0]=3'b000, single address operation; Burst_LEN[2:0]=3'b001,4 address operation; Burst_LEN[2:0]=3'b010,8 address operations; Burst_LEN[2:0]=3'b011,16 address operation; Burst_LEN[2:0]=3'b100,32 address operation, waveform readable only; Burst_LEN[2:0]=3'b101,64 address operation, waveform readable only;	RBUF_DATA	The frame checksum is calculated and emitted by the MKE304T.	Read data from the waveform buffer Burst with the first address {BANK[2:0], REG_ADR[7:0]}.

Checksum algorithm: ADDR+CMD+DATA single-byte summation is negated.

5.4. SPI Write Sequence
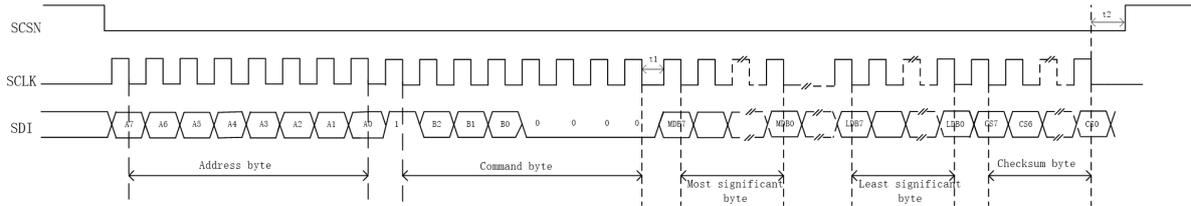
Figure 5-1 SPI write sequence

Working process:

After the SCSN is valid, the host writes the address and command bytes through SPI, and then writes the data bytes. Note:

1．Transmitted in bytes, with the high bit first and the low bit last;

2．Multi-byte registers that transmit high-byte content before low-byte content;

3．The host writes data at the SCLK high level, and the chip takes data on the SCLK falling edge;

4．The time t1 between data bytes should be greater than or equal to half a SCLK period;

5．The last byte of the LSB is transmitted, and the SCSN changes from low to high to end the data transfer. The time t2 between the falling edge of SCLK and the rising edge of SCSN should be greater than or equal to half a SCLK period.

Note: Registers with write-protect functions are written to write-enable commands before the write operation.

5.5. SPI Read Sequence

Working process:

After the host is valid in the SCSN, it first writes the address and command bytes (8bit, including the register address) through SPI, and after the chip receives the read command, the data is output bit by bit from the SDO pin on the rising edge of the SCLK. Note:

1．Passed in bytes, the high bit is first, and the low bit is last;

2．Multi-byte registers that transmit high-byte content before low-byte content;

3．The host writes command bytes at SCLK high level, and the chip reads command bytes on the SCLK falling edge;

4．The chip responds to commands to output data from SDO on the SCLK rising edge;

5．The time t1 of the data byte should be greater than or equal to half a SCLK period;

6．The last byte of the LSB is transmitted, and the SCSN changes from low to high to end the data transfer. The time t2 between the falling edge of SCLK and the rising edge of SCSN should be greater than or equal to half a SCLK period.
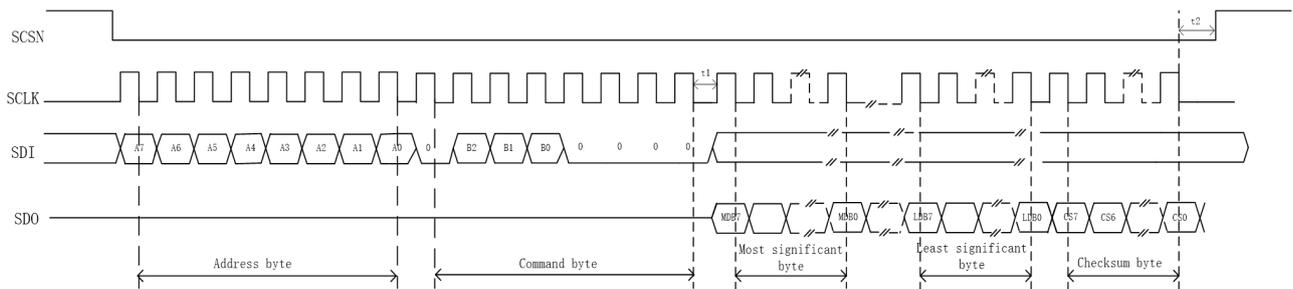
Figure 5-2 SPI read sequence

5.6.SPI Interface Reliability Design

The SPI interface reliability design includes the following aspects:

1．Check function

1) The last byte of the frame structure is the checksum byte of the SPI frame。

2) Checksum of CHECKSUM1(0x6A), CHECKSUM3(0xAE) and NVM1, NVM2 and System Configuration Register checksums CHECKSUM2(0x8B) are available for EMM calibration register and EMM configuration registers.

3) Provides the SPI write check register WData (0x8D) to store the data written by the previous SPI.

2.Write protect function

All readable and writable registers are write-protected.

3.Application circuirt design

The SPI transmission signal line may be jittered due to interference, and the user can filter it according to the external resistance capacitor that needs to be considered. The choice of parameters can be determined as required.

5.7.SPI_burst read note

1. When the address is vacant, burst4/8/16 reads the address register and reads it out as 0;

2. burst read the Bank0 register address out of bounds, you can read the value of the Bank1 address register, because Bank0 is contiguous with the Bank1 address space;

3. When the burst read Bank1 register address crosses the bounds, the out-of-bounds address register reads out to 0 because Bank1 is discontinuous with the waveform buffer address space.

4. When burst4/8/16/32/64 read waveform buffer data address crosses bounds, the out-of-bounds address data readout is 0.

6.HSDC Interface

6.1.Introduction

HSDC is a host interface that follows the SPI protocol, consisting of three wires: HSCSN, HSCLK, HSDAO 3 wires, which only supports sending data to slaves and does not support receiving data.

HSDC is used for waveform buffer data sending, linked with waveform buffer, each time half of the storage space is stored, HSDC interface automatically starts waveform sending, HSCD interface has the following characteristics:

- Only support operation in main mode for waveform buffer data sending

- Clock polarity and clock phase are configurable

- Support transmission rate4.096MHz/2.048MHz/1.024MHz/512KHz

- Support 24bits waveform data expansion to 32bits transmission (high bit supplement 0)

- Support 8bits to accumulate 32bits checksum (not negated)

- Supports CRC16 check (polynomial is $x^{16} + x^{12} + x^5 + 1$)

- Supports transmission of waveform data in reverse byte order

- Supports bitwise reverse order transmission of waveform data

- Configurable delay between data frames by 8 HSCLK clocks

6.2.Waveform Buffer

There is a dedicated waveform storage space inside the chip, the buffer space size is: 128 sample points ×7 channels × 3 bytes = 2688 bytes, by configuring BUFCFG[4:0] = { DMA_WAVECON3 [1], WSAVECON [3:0]} register bits, a variety of waveform storage formats can be realized, and different channel data can be optionally bufferd.

The waveform channel buffer format is divided into: channel chunking buffer mode and channel cross buffer mode

6.2.1.Channel chunking buffer

Configure DMA_WAVECON3. BIT10 = 0, which is the channel chunked buffer mode, and the address mapping is shown in the following figure:

Address Mapping	BANK	{ DMA_WAVECON3 [1]，WSAVECON [3:0]}															Others
		5'b00000/ 5'b011xx	5'b00001	5'b00010	5'b00011	5'b00100	5'b00101	5'b00110	5'b00111	5'b01000	5'b01001	5'b01010	5'b01011	5'b10000	5'b10001	5'b10010	
200H	B2	UA	UA	IA	UA	UB	UC	UA	UB	UC	IA	IB	IC	IN	UA	UA	RESERVED
240H	B2	UA	UA	IA	UA	UB	UC	UA	UB	UC	IA	IB	IC	IN	UA	UA	RESERVED
280H	B2	UB	UA	IA	UA	UB	UC	UA	UB	UC	IA	IB	IC	IN	UC	UB	RESERVED
2C0H	B2	UB	UA	IA	UA	UB	UC	UA	UB	UC	IA	IB	IC	IN	UC	UB	RESERVED
300H	B3	UC	UB	IB	UA	UB	UC	UA	UB	UC	IA	IB	IC	IN	IA	UC	RESERVED
340H	B3	UC	UB	IB	UA	UB	UC	UA	UB	UC	IA	IB	IC	IN	IA	UC	RESERVED
380H	B3	IA	UB	IB	UA	UB	UC	UA	UB	UC	IA	IB	IC	IN	IC	IA	RESERVED
3C0H	B3	IA	UB	IB	UA	UB	UC	UA	UB	UC	IA	IB	IC	IN	IC	IA	RESERVED
400H	B4	IB	UC	IC	IA	IB	IC	UA	UB	UC	IA	IB	IC	IN		IB	RESERVED
440H	B4	IB	UC	IC	IA	IB	IC	UA	UB	UC	IA	IB	IC	IN		IB	RESERVED
480H	B4	IC	UC	IC	IA	IB	IC	UA	UB	UC	IA	IB	IC	IN		IC	RESERVED
4C0H	B4	IC	UC	IC	IA	IB	IC	UA	UB	UC	IA	IB	IC	IN		IC	RESERVED
500H	B5															IN	RESERVED
540H	B5															IN	RESERVED
mode		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

Note: The address in the address mapping column in the table above is the start address of the range.

6.2.2.Channel cross buffer

Configure DMA_WAVECON3. BIT10 = 1, which is the channel cross-buffer mode, and the Address: mapping is shown in the following table.

Address Mapping	{ DMA_WAVECON3 [1]，WSAVECON [3:0]}																		Others
	5'b 00000/ 5'b 011xx	5'h 01	5'h 02	5'h 03	5'h 04	5'h 05	5'h 06	5'h 07	5'h 08	5'h 08	5'h 09	5'h 0A	5'h 10	5'h 11	5'h 12	5'h 13	5'h 14	5'h 15	
200H	UA0	UA0	IA0	UA0	UB0	UC0	UA0	UB0	UC0	IA0	IB0	IC0	IN0	UA0	UA0	UA0	UA0	UA0	RESERVED
201H	UB0	UB0	IB0	IA0	IB0	IC0	UA1	UB1	UC1	IA1	IB1	IC1	IN1	UC0	UB0	IA0	IA0	IA0	
202H	UC0	UC0	IC0	UA1	UB1	UC1	UA2	UB2	UC2	IA2	IB2	IC2	IN2	IA0	UC0	UB0	UC0	UB0	
203H	IA0	UA1	IA1	IA1	IB1	IC1	UA3	UB3	UC3	IA3	IB3	IC3	IN3	IC0	IA0	IB0	IC0	IB0	
204H	IB0	UB1	IB2	UA2	UB2	UC2	UA4	UB4	UC4	IA4	IB4	IC4	IN4	UA1	IB0	UC0	UA1	UC0	
205H	IC0	UC1	IC2	IA2	IB2	IC2	UA5	UB5	UC5	IA5	IB5	IC5	IN5	UC1	IC0	IC0	IA1	IC0	
206H	UA1	UA2	IA2	UA3	UB3	UC3	UA6	UB6	UC6	IA6	IB6	IC6	IN6	IA1	IN0	UA1	UC1	IN0	
⋮	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	
3FF	…	…	…	…	…	…	…	…	…	…	…	…	…	ICn	…	…	ICn	…	

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
H																		
...	...	...	...	...	...	...	...	...	...	...	...	...			...	...		...
4FFH	ICn	UCn	ICn	IAn	IBn	ICn	UAn	UBn	UCn	IAn	IBn	ICn	INn		...	ICn		...
...															...			...
57FH															INn			INn
mode	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17

6.3. HSDC Data Sending

The HSDC interface is linked with the waveform buffer, and the HSDC interface automatically starts waveform transmission each time half of the storage space is stored. The data sending formats supported by the HSDC interface include channel block buffer sending and channel cross-buffer sending, and the data sending format and waveform buffer mode are determined by the DMA_WAVEVON3 register, and the data sending order is described below under different data sending formats.

6.3.1.Channel chunked buffer sending

mode	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14
Buffer the order of the send address in the upper half of the space	200H~23FH ↓ 280H~2BFH ↓ 300H~33FH ↓ 380H~3BFH ↓ 400H~43FH ↓ 480H~4BFH	200H~27FH ↓ 300H~37FH ↓ 400H~47FH		200H~2BFH ↓ 380H~43FH			200H~37FH							200H~23FH ↓ 280H~2BFH ↓ 300H~33FH ↓ 380H~3BFH	200H~23FH ↓ 280H~2BFH ↓ 300H~33FH ↓ 380H~3BFH ↓ 400H~43FH ↓ 480H~4BFH ↓ 500H~53FH
Buffer the order of the send address in the lower half of the space	↓ 240H~27FH ↓ 2C0H~2FFH ↓ 340H~37FH ↓ 3C0H~3FFH ↓ 440H~47FH ↓ 4C0H~4FFH	↓ 280H~2FFH ↓ 380H~3FFH ↓ 480H~4FFH		↓ 2C0H~37FH ↓ 440H~4FFH			↓ 380H~4FFH							↓ 240H~27FH ↓ 2C0H~2FFH ↓ 340H~37FH ↓ 3C0H~3FFH	↓ 240H~27FH ↓ 2C0H~2FFH ↓ 340H~37FH ↓ 3C0H~3FFH ↓ 440H~47FH ↓ 4C0H~4FFH ↓ 540H~57FH

6.3.2.Channel cross buffer sending

mode	0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12	13, 16	14, 17	15
Buffer the order of the send address	200H~37FH	200H~2FFH	200H~3BFH	200H~37FH

in the upper half of the space				
Buffer the order of the send address in the lower half of the space	↓ 380H~4FFH	↓ 300H~3FFH	↓ 3C0H~57FH	↓ 380H~4FFH

6.4. HSDC Interface Sequence

HSDC transmission methods are divided into continuous transmission without delay and transmission with delay.
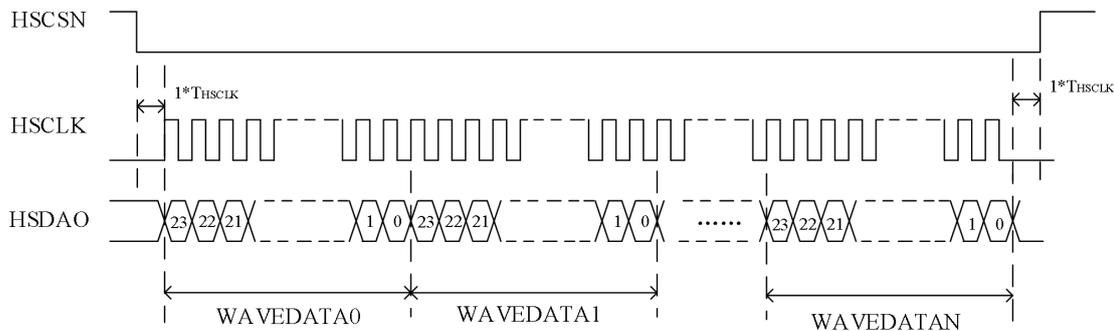
- Continuous transmission mode without delay: the length of each frame data is half of the buffer space data (CRC verification can be configured); At least the time between frames $4*T_{HSCLK}$.

- Delayed transmission mode: the data length of each frame is 8bits/24bits (waveform data expansion enable HSDC_CTL. When BIT11=1, it is 8bits/32bits) can be matched; The interval between frames is $8*T_{HSCLK}$. This mode does not send checksums.

6.4.1. Continuous sending without delay

6.4.1.1. 24-bit raw waveform data sending without check

Configure HSDC_CTL register bit GAP_EN=0, CHK_EN=0, EXT_EN=0, BYTE_INV=0, BIT_INV=0 to enable no verification, no delay, 24-bit raw waveform data, continuous transmission mode, and configure the interface transmission speed and transmission mode, configure EN=1 to enable the HSDC interface. When the waveform buffer module half-total/total interrupt flag is pulled up, the chip select signal HSCSN is pulled low, and the HSDC interface begins to continuously transmit waveform data without delay until all the data in half of the buffer space is sent, and the chip select signal HSCSN is pulled high to stop waveform data transmission.

The following figure shows the specific timing sequence:

No delay, no check, 24-bit raw waveform data, continuous transmission timing diagram (CPOL=0, CPHA=1)

6.4.1.2. 32bits extended waveform data sending without check

Configure HSDC_CTL register bit GAP_EN=0, CHK_EN=0, EXT_EN=1, BYTE_INV=0, BIT_INV=0 to enable no verification, no delay, 32bits extended waveform data, continuous transmission mode, and configure the interface transmission speed and transmission mode; Configure EN=1 to enable the HSDC interface. When the waveform buffer module half-total/total interrupt flag is pulled up, the chip select signal HSCSN is pulled low, and the HSDC interface begins to continuously transmit waveform data without delay until all the data in half of the buffer space is sent, and the chip select signal HSCSN is pulled high to stop waveform data transmission.

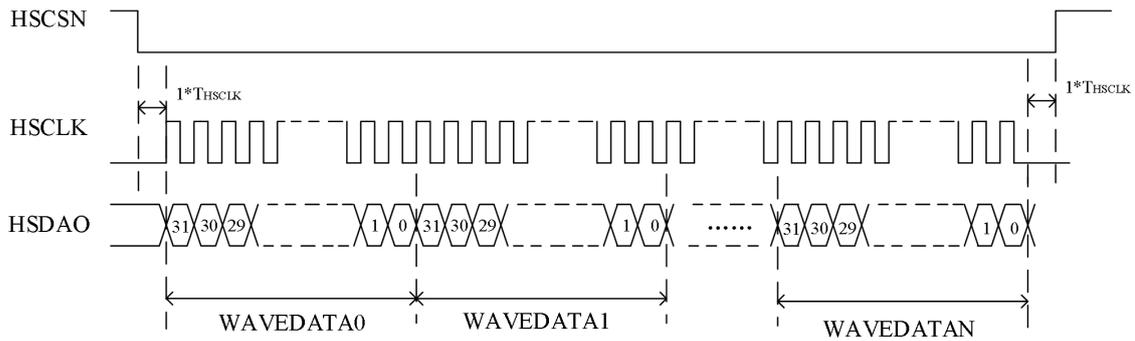The following figure shows the specific timing sequence:

No delay, no check, 32-bit extended waveform data, continuous transmission timing diagram (CPOL=0, CPHA=1)

6.4.1.3.CRC16 check 24bits of raw waveform data sending

Configure HSDC_CTL register bit GAP_EN=0, CHK_EN=1, CHK_SEL=1, EXT_EN=0, BYTE_INV=0, BIT_INV=0 enable CRC check, no delay, 24-bit raw waveform data, continuous transmission mode, and configure the interface transmission speed and transmission mode; Configure EN=1 to enable the HSDC interface. When the waveform buffer module half-total/total interrupt flag is pulled up, the chip select signal HSCSN is pulled low, and the HSDC interface starts to send waveform data until all the data in half of the buffer space is sent, and the CRC check value of the half of the buffer space data (the initial value is 0) is sent. After transmission, the chip select signal HSCSN is pulled high and the waveform output is stopped.
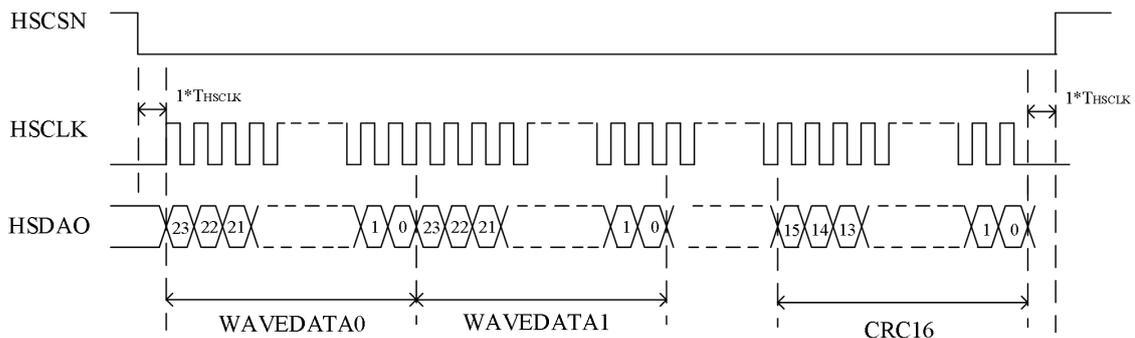
No delay, CRC check, 24-bit raw waveform data, continuous transmission timing diagram (CPOL=0, CPHA=1)

6.4.1.4.CRC16 check 32bits extended waveform data sending

Configure HSDC_CTL register bit GAP_EN=0, CHK_EN=1, CHK_SEL=1, EXT_EN=1, BYTE_INV=0, BIT_INV=0 enable CRC check, no delay, 32-bit extended waveform data, continuous transmission mode, and configure interface transmission speed and transmission mode; Configure EN=1 to enable the HSDC interface. When the waveform buffer module half-total/total interrupt flag is pulled up, the chip select signal HSCSN is pulled low, and the HSDC interface starts to send waveform data until all the data in half of the buffer space is sent, and the CRC check value of the half of the buffer space data (the initial value is 0) is sent. After transmission, the chip select signal HSCSN is pulled high and the waveform output is stopped.

No delay, CRC check, 32-bit extended waveform data, continuous transmission timing diagram (CPOL=0, CPHA=1)
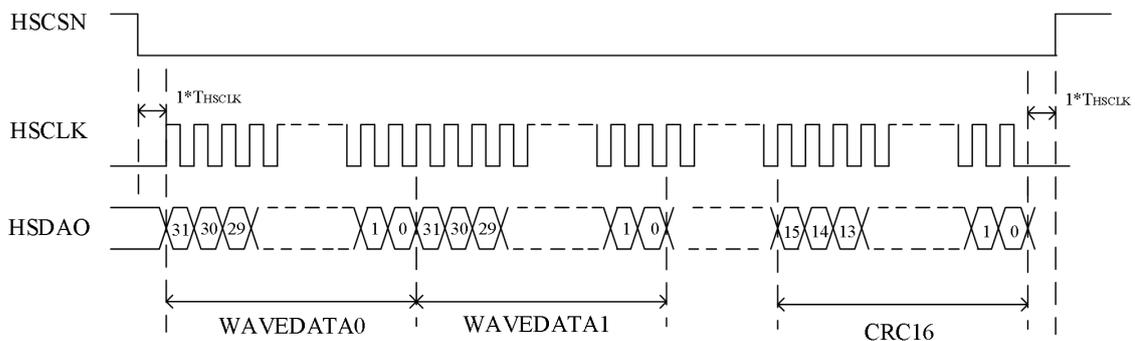
6.4.1.5.Checksum 24-bit raw waveform data sending

Configure HSDC_CTL register bit GAP_EN=0, CHK_EN=1, CHK_SEL=0, EXT_EN=0, BYTE_INV=0, BIT_INV=0 enable checksum, no delay, 24-bit raw waveform data, continuous transmission mode, and configure interface transmission speed and transmission mode; Configure EN=1 to enable the HSDC interface. When the waveform buffer module half-total/total interrupt flag is pulled up, the chip select signal HSCSN is pulled low, and the HSDC interface starts sending waveform data until the data of half of the buffer space is all sent, and the checksum of the half of the buffer space data is sent. After transmission, the chip select signal HSCSN is pulled high and the waveform output is stopped.

No delay, checksum, 24-bit raw waveform data, continuous transmission timing diagram (CPOL=0, CPHA=1)
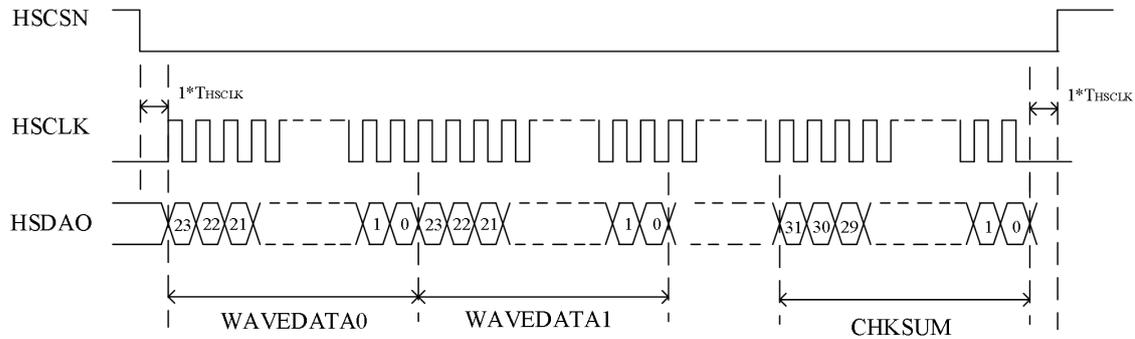
6.4.1.6.Checksum 32bits extended waveform data sending

Configure HSDC_CTL register bit GAP_EN=0, CHK_EN=1, CHK_SEL=0, EXT_EN=1, BYTE_INV=0, BIT_INV=0 to enable checksum, no delay, 32bits extended waveform data, continuous transmission mode, and configure interface transmission speed and transmission mode; Configure EN=1 to enable the HSDC interface. When the waveform buffer module half-total/total interrupt flag is pulled up, the chip select signal HSCSN is pulled low, and the HSDC interface starts sending waveform data until the data of half of the buffer space is all sent, and the checksum of the half of the buffer space data is sent. After transmission, the chip select signal HSCSN is pulled high and the waveform output is stopped.
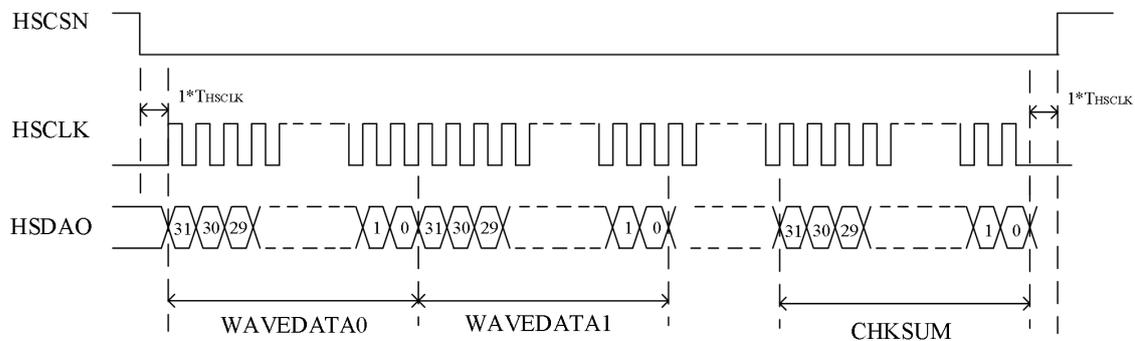
No delay, checksum, 32-bit extended waveform data, continuous transmit timing diagram (CPOL=0, CPHA=1)

6.4.2.Delayed Sending

6.4.2.1.8bits delayed sending

Configure HSDC_CTL register bit GAP_EN=1 (with delay), FWIDTH=0 (frame length 8 bits), EXT_EN=0 (raw waveform data), enable 8-cycle delay transmission between frames with a frame length of 8bits, and configure the interface transmission speed and transmission mode; Configure EN=1 to enable the HSDC interface. When the waveform buffer module half-total/total interrupt flag is pulled up, the HSDC interface chip select signal HSCSN is pulled low and the waveform data and HSCLK clock are started. With 8bit data as a frame, MSB mode is transmitted, that is, the upper 8 bits of the first waveform data are the first frame, the high bit is sent first, and after sending 8bit, HSCSN is pulled high, and HSCLK stops flipping; After the delay of 8*THSCLK cycle, the next frame of data is transmitted, that is, the middle 8 bits of the first waveform data, and the lower 8 bits of data are sent out after the transmission is delayed by 8*THSCLK cycle; And so on to continue sending subsequent

waveform data until the waveform data is sent. If the HSDC module is shut down during transmission, HSCSN is pulled high, the HSCLK clock stops output, and waveform data stops being transmitted.

The following figure shows the specific timing sequence:
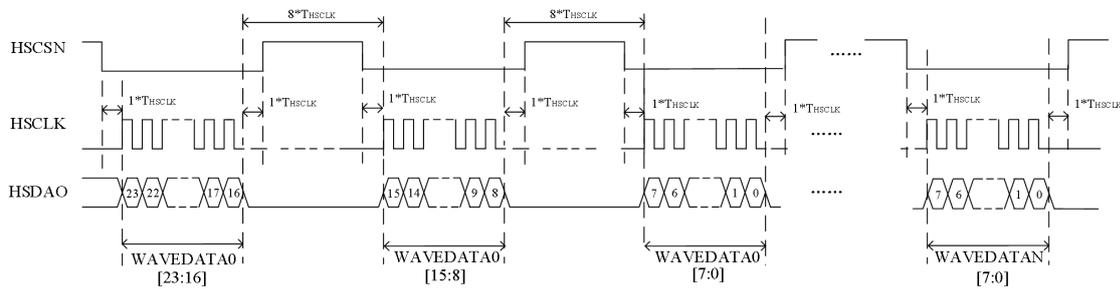
Frame length 8bits, 8cycle delay between frames to send timing diagram (CPOL=0, CPHA=1)

6.4.2.2.24bits/32bits delayed sending

Configure HSDC_CTL register GAP_EN=1 (with delay), FWIDTH = 1 (frame length 24 bits or 32 bits, EXT _EN=0 is 24bits, EXT_EN=1 is 32bits), enable 8cycle delay transmission between frames with a frame length of 24bits/32bits, and configure the interface transmission speed and transmission mode; Configure EN=1 to enable th e HSDC interface. When the waveform buffer module half-total/total interrupt flag is pulled up, the HSDC interfa ce chip select signal HSCSN is pulled low and the waveform data and HSCLK clock are started. With 24-bit/32-bi t data as a frame, MSB mode is sent, each frame of data is sent, HSCSN is raised, and the delay between frames is 8*THSCLK clock cycle; HSCSN pulls low again and continues to transmit the next frame of waveform data until the waveform data is sent. If the HSDC module is shut down during transmission, HSCSN is pulled high, the HS CLK clock stops output, and waveform data stops being transmitted.

The following figure shows the specific timing sequence:
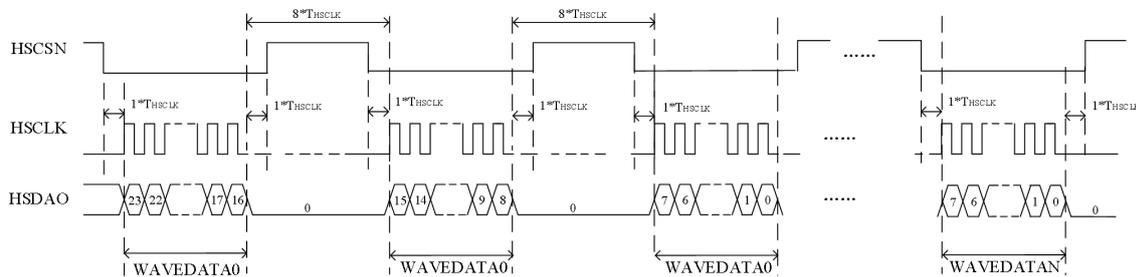
Original waveform data frame length 24 bits between frames 8cycle delay transmission timing diagram (CPOL=0, CPHA=1)
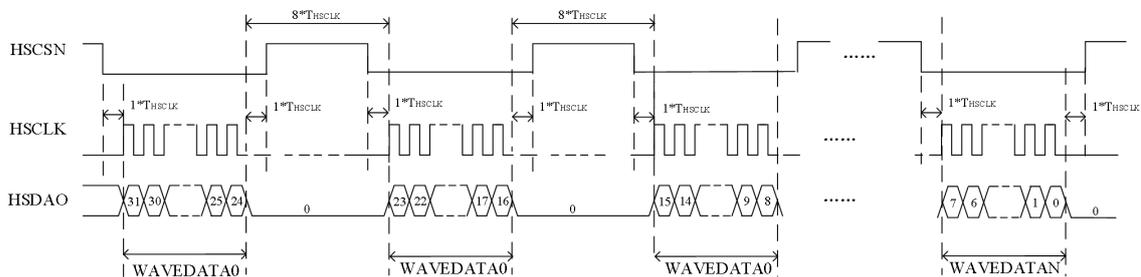
Extended waveform data frame length 32 bits between frames 8cycle delay transmission timing diagram (CPOL=0, CPHA=1)

6.5.HSDC flow of usage

1. Configure HSDC_CTL registers, HSDC transmission speed, transmission mode, etc;

2. Configure EMMIE2 [12:11] as required, HSDC error interrupt, HSDC output half-block buffer interrupt e nabled;

3. Configure HSDC_CTL.EN=1 to enable HSDC interface;

4. Configure WSAVECON[5:4] (Mode 0) or DMA_WAVECON3[0] (Mode 1 and Mode 2) waveform buffer enabled, see Section 2.4.2 for additional configuration of waveform buffer. After the waveform buffer module buffer is half total, HSDC automatically sends the waveform, and the BUS position 1 during the data transmission period; After half of the storage space is output, the BUS bit is cleared to zero, and the output waveform data is paused. If interrupt enable is configured EMMIE2.HSDC_TWAVE_HIE=1, the output interrupt.

5. When no send is required, configure the HSDC_CTL register bit EN=0 to shut down the HSDC interface.

6.6. Analysis of waveform data volume and HSDC rate

The amount of waveform data in different scenarios and the minimum HSCLK frequency required for different output modes are shown below:

6.6.1. 24-bit raw waveform data application scenario

Formula for calculating the amount of waveform data:

$$\text{Date size} = (n*f*ch*24) \text{ bit/s}$$

➢ Number of per cycle points: n

➢ Work frequency: f

➢ Channel number: ch

Note: In practice, the HSDC rate configuration is greater than or equal to the rate described in the following table.

Points number of cycles n	Frequency f	Buffer channel number ch	Date size (bit/s)	HSDC rate		
				Continue mode	24bit delayed output	8bit delayed output
128 points	50Hz	7 channels	1.075M	2.048M	2.048M	4.096M
128 points	50Hz	6 channels	0.922M	1.024M	2.048M	2.048M
128 points	50Hz	4 channels	0.614M	1.024M	1.024M	2.048M
128 points	50Hz	3 channels	0.461M	0.512M	1.024M	1.024M
128 points	50Hz	2 channels	0.307M	0.512M	0.512M	1.024M
128 points	50Hz	1 channel	0.124M	0.512M	0.512M	0.512M
256 points	50Hz	7 channels	2.151M	4.096M	4.096M	not supported
256 points	50Hz	6 channels	1.844M	2.048M	4.096M	4.096M
256 points	50Hz	4 channels	1.229M	2.048M	2.048M	4.096M
256 点	50Hz	3 channels	0.922M	1.024M	2.048M	2.048M
256 points	50Hz	2 channels	0.615M	1.024M	1.024M	2.048M

256 points	50Hz	1 channel	0.307M	0.512M	0.512M	1.024M
512 points	50Hz	7 channels	4.301M	not supported	not supported	not supported
512 points	50Hz	6 channels	3.687M	4.096M	not supported	not supported
512 points	50Hz	4 channels	2.458M	4.096M	4.096M	not supported
512 points	50Hz	3 channels	1.843M	2.048M	4.096M	4.096M
512 points	50Hz	2 channels	1.229M	2.048M	2.048M	4.096M
512 points	50Hz	1 channel	0.614M	1.024M	1.024M	2.048M
128 points	60Hz	7 channels	1.291M	2.048M	2.048M	4.096M
128 points	60Hz	6 channels	1.106M	2.048M	2.048M	4.096M
128 points	60Hz	4 channels	0.737M	1.024M	1.024M	2.048M
128 points	60Hz	3 channels	0.553M	1.024M	1.024M	2.048M
128 points	60Hz	2 channels	0.369M	0.512M	0.512M	1.024M
128 points	60Hz	1 channel	0.184M	0.512M	0.512M	0.512M
256 points	60Hz	7 channels	2.581M	4.096M	4.096M	not supported
256 points	60Hz	6 channels	2.212M	4.096M	4.096M	not supported
256 points	60Hz	4 channels	1.475M	2.048M	2.048M	4.096M
256 points	60Hz	3 channels	1.106M	2.048M	2.048M	4.096M
256 points	60Hz	2 channels	0.738M	1.024M	1.024M	2.048M
256 points	60Hz	1 channel	0.369M	0.512M	0.512M	1.024M
512 points	60Hz	7 channels	5.161M	not supported	not supported	not supported
512 points	60Hz	6 channels	4.424M	not supported	not supported	not supported
512 points	60Hz	4 channels	2.949M	4.096M	4.096M	not supported
512 points	60Hz	3 channels	2.212M	4.096M	4.096M	not supported
512 points	60Hz	2 channels	1.475M	2.048M	2.048M	4.096M
512 points	60Hz	1 channel	0.737M	1.024M	1.024M	2.048M

6.6.2.32bits expand waveform data application scenarios

Waveform data quantity calculation formula:

$$\text{Data size} = (n*f*ch*32) \text{ bit/s}$$

➢Number of per cycle points: n

➢Work frequency: f

➢Channel number: ch

Note: In practice, the HSDC rate configuration is greater than or equal to the rate described in the following table.

Points number of cycles n	Frequency f	Buffer channel number ch	Date size (bit/s)	HSDC rate		
				Continue mode	32bit delayed output	8bit delayed output
128 points	50Hz	7 channels	1.433M	2.048M	2.048M	4.096M
128 points	50Hz	6 channels	1.229M	2.048M	2.048M	4.096M
128 points	50Hz	4 channels	0.819M	1.024M	2.048M	2.048M
128 points	50Hz	3 channels	0.615M	1.024M	1.024M	2.048M
128 points	50Hz	2 channels	0.409M	0.512M	1.024M	1.024M
128 points	50Hz	1 channel	0.165M	0.512M	0.512M	0.512M
256 points	50Hz	7 channels	2.868M	4.096M	4.096M	not supported
256 points	50Hz	6 channels	2.459M	4.096M	4.096M	not supported
256 points	50Hz	4 channels	1.639M	2.048M	4.096M	4.096M
256 points	50Hz	3 channels	1.229M	2.048M	2.048M	4.096M
256 points	50Hz	2 channels	0.820M	1.024M	2.048M	2.048M
256 points	50Hz	1 channel	0.409M	0.512M	1.024M	1.024M
512 points	50Hz	7 channels	5.735M	not supported	not supported	not supported
512 points	50Hz	6 channels	4.916M	not supported	not supported	not supported
512 points	50Hz	4 channels	3.277M	4.096M	not supported	not supported
512 points	50Hz	3 channels	2.457M	4.096M	4.096M	not supported
512 points	50Hz	2 channels	1.639M	2.048M	4.096M	4.096M
512 points	50Hz	1 channel	0.819M	1.024M	2.048M	2.048M

128 points	60Hz	7 channels	1.721M	2.048M	4.096M	4.096M
128 points	60Hz	6 channels	1.475M	2.048M	2.048M	4.096M
128 points	60Hz	4 channels	0.983M	1.024M	2.048M	2.048M
128 points	60Hz	3 channels	0.737M	1.024M	1.024M	2.048M
128 points	60Hz	2 channels	0.492M	0.512M	1.024M	1.024M
128 points	60Hz	1 channel	0.245M	0.512M	0.512M	0.512M
256 points	60Hz	7 channels	3.441M	4.096M	not supported	not supported
256 points	60Hz	6 channels	2.949M	4.096M	4.096M	not supported
256 points	60Hz	4 channels	1.967M	2.048M	4.096M	4.096M
256 points	60Hz	3 channels	1.475M	2.048M	2.048M	4.096M
256 points	60Hz	2 channels	0.984M	1.024M	2.048M	2.048M
256 points	60Hz	1 channel	0.492M	0.512M	1.024M	1.024M
512 points	60Hz	7 channels	6.881M	not supported	not supported	not supported
512 points	60Hz	6 channels	5.899M	not supported	not supported	not supported
512 points	60Hz	4 channels	3.932M	4.096M	not supported	not supported
512 points	60Hz	3 channels	2.949M	4.096M	4.096M	not supported
512 points	60Hz	2 channels	1.967M	2.048M	4.096M	4.096M
512 points	60Hz	1 channel	0.983M	1.024M	2.048M	2.048M

6.7. HSDC Register Description

6.7.1.HSDC_CTL

Address: C9H; Word length: 4 bytes; Default: 0x04;

The HSDC_CTL register adds a configuration register for the high-speed SPI interface of the waveform buffer output to the RA9302B, HSDC. This register is controlled by an EMU clock, not an HSDC clock.

Bit(s)	Name	Description	R/W	Reset
31:9	Reserved	Reserved	RO	0
12	BIT_INV	The transmit waveform is enabled in reverse bit order.	RW	0

		=0: disabled =1: enabled		
11	EXT_EN	Send waveform data extension enable: =0: Send raw 24-bit waveform data =1: Send 32-bit extended waveform data (high octet 0)	RW	0
10	BYTE_INV	The output waveform data is enabled in byte reverse order: =0: disabled =1: enabled	RW	0
9	CHK_SEL	Check mode configuration: =0:8-bit checksum calculation, the result is 32-bit, no negation =1:16-bit CRC check calculation	RW	0
8	GAP_EN	Frame delay selection =0: no delay =1: delay $8*T_{HSCLK}$	RW	0
7	FWIDTH	Interface frame length selection: =0:8bit =1:24bit Only valid when there is a delay in sending.	RW	0
6:4	CLKDIV	HSCLK Clock division factor formula: $f_{HSCLK}=f_{sysclk}/ (2^{\wedge} (CLKDIV+1))$ =3'b000HSCLK frequency is 4.096MHz =3'b001HSCLK frequency is 2.048MHz =3'h010HSCLK frequency is 1.024MHz =3'h011HSCLK frequency is 0.512MHz =others HSCLK frequency is 4.096MHz Note: f_{sysclk} is system clock 8.192MHz	RW	0
3	CHK_EN	=1: Check digit required =0: No check digit required Valid only when sent consecutively	RW	0
2	CPHA	HSDC Clock phase selection =0: leading edge sampling data	RW	1

		=1: leading edge setup data			
1	CPOL	HSDC Clock polarity selection =0: "HSCLK" is set low on idle = 1: "HSCLK" is set high in idle state	RW	0
0	EN	Interface enable bit =0: Disable HSDC interface =1: Enable HSDC interface EMUIF2. HSDC_ERR_IF=1, the register bit is automatically cleared.	RW	0

Note:

1. The parameters of this register can only be configured when HSDC_EN = 0;

2. Example illustration of waveform data sending after multiple configurations:

BIT_INV	EXT_EN	BYTE_INV	Data (Send order: left to right)	Note
0	0	0	{data[23:16],data[15:8],data[7:0]}	Original waveform data
1	0	0	{data[0:7],data[8:15],data[16:23]}	Bitwise reverse order
0	0	1	{data[7:0], data[15:8], data[23:16]}	Byte reverse order
1	0	1	{data[16:23],data[8:15],data[0:7]}	Byte reverse and bitwise reverse
0	1	0	{8'h0,data[23:16],data[15:8],data[7:0]}	Waveform data expansion
1	1	0	{data[0:7],data[8:15],data[16:23],8'h0}	Expanded in bitwise order
0	1	1	{data[7:0],data[15:8],data[23:16],8'h0}	Expanded in reverse byte order
1	1	1	{8'h0,data[16:23],data[8:15],data[0:7]}	Expanded in reverse byte order and bitwise reverse order

6.7.2.HSDC_CRC

Address: CAH; Word length: 4bytes; Default: 0x0.

When any parameter configuration of the HSDC interface, the HSDC_CRC module performs CRC16 checksum or checksum calculation on the output waveform, and the verification result is stored in the HSDC_CRC register, and the check result register is updated every half of the memory length data, and the initial value of the register is 0 each time it is updated.

Bit(s)	Name	Description	R/W	Reset

| 31:0 | RESULT | Stores CRC16 checksum or 8-bit checksum results:

If HSDC_CTL. If CRC16 is selected for BIT9=1, the check result is stored in the lower 16 bits of this register;

If HSDC_CTL. If BIT9=0 selects an 8-bit checksum, the 32-bit result is stored in this register. | RO | ---- |

7.Automatic temperature Offset metering accuracy module

7.1.Features

✓Internal SARADC & TPS unit, temperature measurement accuracy < 2°C

✓Supports UA/UB/UC/IA/IB/IC/IN 7 channels of automatic temperature compensation

✓Each channel has independent compensation coefficients for high temperature and low temperature segment

✓Support three working modes: manual mode, single automatic mode, cyclic automatic mode, among which the cyclic automatic mode can realize temperature compensation without software intervention

✓Cyclic automatic mode temperature compensation cycle 1S-256S can be configured

✓Support temperature stabilization function, |two temperature measurement temperature difference|> set temperature threshold to start the calculation of temperature compensation gain coefficient

✓It supports temperature protection function near 25°C, and the temperature protection area can be configured

✓Support temperature out-of-bounds protection function, the lower temperature limit of temperature compensation and upper temperature can be configured, and you can choose whether to calculate temperature compensation and update the ECT temperature compensation gain register when the temperature exceeds the boundary

✓Support error out-of-bounds protection function, error out-of-bounds threshold can be configured, support error out-of-bounds alarm interrupt, out-of-bounds temperature compensation gain coefficient is not updated to the EMU channel temperature compensation gain factor register

✓ Supports interrupt of ECT warm-compensated gain factor updates.

7.2.Description

See *Micro Application Note* and *Micro library Functions*.

7.3.Register

7.3.1.Register List

Note: The registers of the automatic temperature compensation metering accuracy module are all located under the bank0 address

Address	Name	R/W	Length	Deault	Description
D0H	ECT_WREN	R/W	4	0x0	Error temperature compensated configuration register write enable
D1H	SAR_CTL0	R/W	4	0x8787CC14	SAR control register 0 (recommended 0x8787CE10)
D2H	SAR_CTL1	R/W	4	0x0	SAR control register 1
D3H	Reserved	----	--	----	Reserved
D4H	TEMP_OS	R/W	4	0x0	Temperature OFFSET Register

D5H	ECT_CTL	R/W	4	0x0	Error temperature compensation control register
D6H	ECT_CMD_STA	R/W	4	0x0	Error temperature compensation command status register
D7H	ECT_LT_SET	R/W	4	0x03600014	Error temperature compensated low temperature segment offset temperature threshold register
D8H	ECT_HT_SET	R/W	4	0x01540014	Error temperature compensated temperature threshold register for high temperature section
D9H	ECT_Timer_SET	R/W	4	0x9	Error temperature offset cycle setting
DAH	ECT_PROTECT_TEMP	R/W	4	0x8	Error temperature offset temperature protection zone setting
DBH	ECT_PROTECT_IGAIN	R/W	4	0x147	I-channel error temperature offset error protection zone setting
DCH	ECT_PROTECT_UGAIN	R/W	4	0x147	U-channel error temperature offset error protection zone setting
DDH	ECT_PROTECT_INGAIN	R/W	4	0x147	IN channel error temperature offset error protection zone setting
DEH	ECT_LT_KIA	R/W	4	0x0	Automatic temperature offset linear fitting coefficient for IA channel error in low temperature segment
DFH	ECT_LT_KIB	R/W	4	0x0	Automatic temperature offset linear fitting coefficient for IB channel error in low temperature range
E0H	ECT_LT_KIC	R/W	4	0x0	Automatic temperature offset linear fitting coefficient for IC channel error in low temperature segment
E1H	ECT_LT_KUA	R/W	4	0x0	Automatic temperature offset linear fitting coefficient of UA channel error in low temperature section
E2H	ECT_LT_KUB	R/W	4	0x0	Automatic temperature offset linear fitting coefficient of UB channel error in low temperature section
E3H	ECT_LT_KUC	R/W	4	0x0	Automatic temperature offset linear fitting coefficient of UC channel error

					in low temperature section
E4H	ECT_LT_KIN	R/W	4	0x0	Automatic temperature offset linear fitting coefficient for IN channel error in low temperature segment
E5H	ECT_HT_KIA	R/W	4	0x0	Automatic temperature offset linear fitting coefficient for IA channel error in high temperature range
E6H	ECT_HT_KIB	R/W	4	0x0	Automatic temperature offset linear fitting coefficient for IB channel error in high temperature range
E7H	ECT_HT_KIC	R/W	4	0x0	Automatic temperature offset linear fitting coefficient for IC channel error in high temperature range
E8H	ECT_HT_KUA	R/W	4	0x0	Automatic temperature offset linear fitting coefficient for UA channel error in high temperature section
E9H	ECT_HT_KUB	R/W	4	0x0	Automatic temperature offset linear fitting coefficient for UB channel error in high temperature section
EAH	ECT_HT_KUC	R/W	4	0x0	Automatic temperature offset linear fitting coefficient for UC channel error in high temperature section
EBH	ECT_HT_KIN	R/W	4	0x0	Automatic temperature offset linear fitting coefficient for IN channel error in high temperature section
ECH	ECT_TEMP	R/W	4	0x0	This automatic temperature supplement temperature measurement
EDH	ECT_RESULT_WREN	R/W	4	0x0	Error temperature result register write enabled
EEH	ECT_IAGAIN	R/W	4	0x0	IA channel error temperature offset gain
EFH	ECT_IBGAIN	R/W	4	0x0	IB channel error temperature offset gain
F0H	ECT_ICGAIN	R/W	4	0x0	IC channel error temperature offset gain
F1H	ECT_UAGAIN	R/W	4	0x0	UA channel error temperature offset gain

F2H	ECT_UBGAIN	R/W	4	0x0	UB channel error temperature offset gain
F3H	ECT_UCGAIN	R/W	4	0x0	UC channel error temperature offset gain
F4H	ECT_INGAIN	R/W	4	0x0	IN channel error temperature offset gain
F5H	ECT_TEMP_UD	R/W	4	0x64	The temperature value for the temperature offset coefficient was recently updated
F6H	SARADC_TADJ	R/W	4	0x0683_0111	SAR ADC calibration register (recommended 0x0699_4311)
F7H	SARADC_TEMP	R	4	----	SAR ADC temperature measurement output register
F8H	SAR_EN	R/W	1	0x0	SAR ADC enable register

7.3.2. Description

7.3.2.1. Write enable register

7.3.2.1.1. ECT_WREN register (0xD0)

Address: D0H; Word length: 4 bytes; Default: 0x00.

This register is used for partial error temperature offset module readable and writable registers, write protection, and write enable. After power-on reset and software reset, the register returns to the default write-protected state. Protected address: bank0: D4H~EBH, F7H;

Bit(s)	Name	Description	R/W	Reset
31:8	Reserved	Reserved	RO	0
7:0	WREN	=0xEA, error temperature offset module bank0 D4H~EBH, F7H write enable; = 0x0, the above register write protection; = Other value, invalid.	RW	0

7.3.2.1.2. SAR_CTL0 register (0xD1)

Address: D1H; Word length: 4 bytes; Default: 0x8787CC14.

This register is used for SAR ADC temperature measurement configurations such as channel selection, gain adjustment, etc. The recommended value for internal temperature measurement is 0x8787CE10.

Bit(s)	Name	Description	R/W	Reset
31:23	Reserved	Reserved	RW	0x10F

Bit(s)	Name	Description	R/W	Reset
22:19	CHSEL	Temperature measurement channel selection: =0x0, internal temperature sensor temperature measurement; =0x7, reserve =0x8, reserve; = Other value, invalid.	RW	0
18:16	PGA_GAIN	Gain factor adjustment: =0x0, input signal size multiplied by 0.125 times; = 0x1, the input signal size multiplied by 0.25 times; = 0x2, the input signal size multiplied by 0.375 times; = 0x3, the input signal size multiplied by 0.5 times; =0x4, the input signal size multiplied by 0.625 times; = 0x5, the input signal size multiplied by 0.75 times; = 0x6, input signal size multiplied by 0.875 times; = 0x7, the input signal size multiplied by 1 times;	RW	0x7
15:0	Reserved	Reserved. Recommend to change to 0xCE10.	RW	0xCC14

7.3.2.1.3. SAR_CTL1 register (0xD2)

Address: D2H; Word length: 4 bytes; Default: 0x0.

This register is used to initiate the SAR ADC temperature measurement.

Bit(s)	Name	Description	R/W	Reset
31:2	Reserved	Reserved	RO	0x0
1	SAR_AO	SAR opening mode selection: =0, indicating that SAR is turned on intermittently (KICK is enabled once at a time); =1, indicating that the SRA is normally open (for automatic temperature measurement by ECT	RW	0

		hardware).		
0	KICK	Write 1 to start a temperature measurement, write 0 is invalid. Note: After the ECT hardware automatic temperature measurement is started, the KICK is invalid.	WO	0

7.3.2.1.4. TEMP_OS register (0xD4)

Address: D0H; Word length: 4 bytes; Default: 0x00.

This register is used for temperature offset calibration.

Bit(s)	Name	Description	R/W	Reset
31:6	Reserved	Reserved	RO	0
5:0	TEMP_OS	When a single or cyclic auto temperature compensation occurs, the temperature register ECT_TEMP = TEMP + TEMP_OS is TEMP_OS signed number. This register is in twos complement format, BIT5 is the sign bit, the correction scale is 0.25°C, to make the temperature value change t (°C), it should be filled in TEMP_OS = t * 4; Calibration temperature range:-8°C~ + 7.75°C	RW	0

7.3.2.1.5. ECT_CTL register (0xD5)

Address: D5H; Word length: 4 bytes; Default: 0x00.

Bit(s)	Name	Description	R/W	Reset
31:13	Reserved	Reserved	RO	0
12	TEMPEL_PROTECT_EN	Temperature out-of-bounds protection function enable bit: = 1, turn on the temperature out-of-bounds protection function; = 0 to turn off the temperature out-of-bounds protection function.	RW	0
11	TEMPEL_GAIN CAL_EN	When the temperature out-of-bounds event occurs, the temperature- offset gain coefficient calculates the enabling bit: = 1, and when the temperature out-of-	RW	0

		bounds event occurs, the calculation engine does not calculate the temperature offset gain coefficient, but only reports the temperature out-of-bounds event; = 0, when the temperature out-of-bounds event occurs, not only the temperature out-of-bounds event is reported, but also the calculation engine is started to calculate the temperature offset gain coefficient, and the corresponding temperature offset gain coefficient register is written to the corresponding temperature offset gain factor register and the corresponding bit assert ECT_CMD_STA [10:4] is triggered. Note: This configuration bit is only valid when ECT_CTL[12] = 1.		
10	ERREL_PROTE CT_EN	Enabling bit of temperature offset error out-of-bounds protection function: = 1, enable the temperature offset error out-of-bounds protection function; = 0 to disable the temperature offset error out-of-bounds protection function.	RW	0
9	TEMP_PROTE CT_EN	Temperature offset zone protection function enable bit: = 1, turn on the temperature offset zone protection function; = 0 to disable the temperature offset zone protection function.	RW	0
8:2	CH_SEL[6:0]	Channel selection register bits: = 1, select { IN, UC, UB, UA, IC, IB, IA } CHANNEL AUTO TEMPERATURE COMPENSATION; = 0, do not select { IN, UC, UB, UA, IC, IB, IA } channel automatic temperature compensation	RW	0
1:0	ECT_MODE	00: Manual mode; Only the temperature offset gain registers function and are software configurable. The auto-temperature offset register and compute module are not working. 01: Semi-automatic mode; The automatic temperature offset register and the calculation module are enabled, the ECT_Timer_SET register is invalid, the ECT_TEMP register is readable and writable, the SARADC temperature	RW	0

measurement fails, and after starting, the hardware writes the temperature according to the ECT_TEMP, and performs a single automatic temperature offset, if the temperature offset conditions are met, the temperature offset gain register is automatically adjusted once.

10: Single automatic temperature offset mode; The automatic temperature offset register and the calculation module are enabled, ECT_Timer_SET the register is invalid, only a single automatic temperature offset is performed after starting, and if the temperature offset condition is met, the temperature offset gain register is automatically adjusted once.

11: Cyclic automatic temperature offset mode; Automatic temperature offset registers and calculation modules are enabled. Set the cycle by ECT_Timer_SET register to automatically cycle the temperature offset. If the temperature offset condition is met, the temperature offset gain register period is automatically adjusted.

7.3.2.1.6. ECT_CMD_STA register (0xD6)

Address: D6H; Word length: 4 bytes; Default:0x00.

Bit(s)	Name	Description	R/W	Reset
31:20	Reserved	Reserved	RO	0
19:13	ERREL_IF[6:0]	{IN, UC, UB, UA, IC, IB, IA} channel auto-temperature offset error out-of-bounds flag. When the temperature offset error protection function is enabled, if the gain coefficient of the high temperature segment or low temperature segment of a channel calculated by the calculation module exceeds the threshold set by ECT_PROTECT_xxGAIN, an error out-of-bounds event occurs for the channel. When an error out-of-bounds event occurs on a channel, the channel error out-of-bounds flag is set. Either bit flag assert causes the EMMIF2.AUTOECT_ERREL_IF to assert, and if EMMIE2.AUTOECT_ERREL_IE interrupt is enabled, any bit flag assertion will produce AUTOECT_ERREL interrupt. ERREL_IF [6:0] Write 1 to clearance for each sign, write 7FH to clear all bits and clear EMMIF2.AUTOECT_ERRIF sign at	W1C	0

		the same time to clear the break.		
12	TEMPEL_IF	Automatic temperature offset out-of-bounds event flag. When the automatic temperature offset out-of-boundary protection function is enabled, a temperature out-of-bounds event occurs when the upper limit of the automatic temperature offset set by the detection temperature ECT_TEMP>ECT_HT_UL or the lower limit of the automatic temperature offset set by the detection temperature ECT_TEMP<ECT_LT_LL is detected. In the event of a temperature out-of-bounds event, ECT_CTL [11] can be used to choose whether to stop the automatic temperature offset calculation and set the flag in position. This bit is written 1 and cleared zero.	W1C	0
11	TEMP_PROTECT_IF	Automatic temperature offset temperature protection event flag. When the automatic temperature offset temperature protection function is turned on, if | Temperature detected - 25°C | When the set protection temperature threshold is <, an automatic temperature offset protection event occurs. This event causes the ECT to stop the calculation of the automatic thermal offset coefficient, clearing the resulting register ECT_xxGAIN and asserting the flag TEMP_PORTECT_IF. If the zeroing action causes the ECT_xxGAIN to be updated, the ECT_TEMP_UD is updated to the current detection temperature value, ECT_CMD_STA. GAINUD_IF [6:0] the corresponding channel flag is also set. The flag writes 1 and cleared 0.	W1C	0
10:4	GAINUD_IF[6:0]	{IN, UC, UB, UA, IC, IB, IA} channel temperature compensation gain factor adjustment flag. After starting a single automatic temperature offset or cyclic automatic offset mode, this register bit indicates whether the automatic offset updates the temperature offset gain factor of the corresponding channel. =1, indicating that the corresponding channel of this temperature measurement meets the temperature offset gain coefficient adjustment conditions, and the gain factor register ECT _xxGAIN of this channel has been updated to the temperature offset	W1C	0

		calculation result.		
		=0, which means that the corresponding channel of this temperature measurement does not meet the temperature offset gain coefficient adjustment conditions, and the gain factor register ECT _xxGAIN of the channel has not been updated. Asserting any bit of the flag causes the EMMIF2.AUTOECT_GAINUDIF to be asserted, and if EMMIE2.AUTOECT_GAINUDIE interrupt is enabled, any bit of the flag asserting will cause a AUTOECT_GAINUD interrupt. GAINUD_IF [6:0] Write 1 and clear, write 7FH to clear all bits and clear EMMIF2 for each sign. AUTOECT_GAINUDIF flag clears the interrupt at the same time.		
3:0	CMD_STA	Hardware temperature offset boot command register bits: Write: 1) Write 0xA, start hardware temperature offset; 2) Write 0x3, turn off hardware temperature offset, the resulting register ECT_xxGAIN, ECT_TEMP_UD cleared, other configuration registers are retained. Write other values is invalid. Read: 1) If the single automatic temperature offset mode is started, read as 0xB, indicating busy, and read 0, indicating the end of this temperature offset. 2) If the startup cycle automatically makes up the temperature, it is read as 0xB, which means busy; Reading 0 indicates that this temperature offset is over, and the next round of temperature offset after the set timer is ready. 3) If the semi-automatic temperature offset mode is started, it is read as 0xB, which means busy; Read 0 to indicate that this warming is over, wait for the next manual start of the hardware warming. 4) If the automatic temperature offset and reset commands are turned off, the value read is always 0.	RW	0

7.3.2.1.7. ECT_LT_SET register (0xD7)

Address: D7H; Word length: 4 bytes; Default: 0x03600014.

Bit(s)	Name	Description	R/W	Reset
31:26	Reserved	Reserved	RO	0
25:16	ECT_LT_LL	The lower temperature limit of the error temperature offset in the low temperature segment (less than 25 °C is the low temperature segment, the same below) is lower than the temperature point, and the automatic temperature offset is stopped. The default is -40°C binary code.	RW	0x360
15:10	Reserved	Reserved	RO	0
9:0	ECT_LT_GAP	Low temperature segment interval, automatic temperature offset unit according to the set cycle timing detection temperature, when the detection temperature is in the low temperature segment (< 25 °C), meet |current detection temperature - last temperature offset |≥ECT_LT_GAP, start automatic temperature offset, otherwise, keep the last temperature offset result is not updated. The default is a binary code of 5°C.	RW	0x14

7.3.2.1.8.ECT_HT_SET register (0xD8)

Address: D8H; Word length: 4 bytes; Default: 0x01540014.

Bit(s)	Name	Description	R/W	Reset
31:26	Reserved	Reserved	RO	0
25:16	ECT_HT_UL	High temperature segment (≥ 25 °C for high temperature segment, the same below) error temperature offset temperature upper limit value configuration, if AUTOECT_TEMP_EL enabled, the detection temperature is higher than the temperature point, automatic temperature compensation temperature out of bounds event occurs. The default is a binary code of 85°C.	RW	0x154
15:10	Reserved	Reserved	RO	0
9:0	ECT_HT_GAP	High temperature section error temperature compensation temperature interval. The automatic temperature compensation unit detects the temperature regularly according to the set cycle, and when the detection temperature is in the low temperature section (≥ 25°C), the threshold temperature set by the ≥EDT_HT_GAP detection temperature - last compensation temperature is met, the automatic temperature compensation is started. The default is a binary code of 5°C.	RW	0x14

7.3.2.1.9.ECT_Timer_SET register (0xD9)

Address: D9H; Word length: 4 bytes; Default: 0x9.

Bit(s)	Name	Description	R/W	Reset
31:8	Reserved	Reserved	RO	0
7:0	ECT_Timer_Cyc	Unit: s, after starting the automatic temperature offset, the automatic temperature offset, unit detects the temperature according to the *(register + 1)* s cycle timer set by the register, default: 0x9. It can be set up to 256s.	RW	0x9

7.3.2.1.10.ECT_PROTECT_TEMP register (0xDA)

Address: DAH; Word length: 4 bytes; Default: 0x08.

Bit(s)	Name	Description	R/W	Reset
31:10	Reserved	Reserved	RO	0
9:0	ECT_PROTECT_TEMP	Automatic temperature offset temperature protection area setting. When the AUTOECT_TEMP_PORTECT_EN is enabled, if the detected temperature is -25°C|< set the protection temperature threshold, the automatic temperature offset protection event is triggered. The default setting is 2°C, which means that the detection temperature is within 25±2°C to trigger a temperature protection event.	RW	Binary code at 2 °C

7.3.2.1.11.ECT_PROTECT_IGAIN register (0xDB)

Address: DBH; Word length: 4 bytes; Default: 0x147;

Bit(s)	Name	Description	R/W	Reset
31:16	Reserved	Reserved	RO	0
15:0	ECT_PROTECT_IGAIN	Automatic temperature offset error protection threshold setting. When *| the current channel gain factor (ECT_ IxGAIN) offset by the current channel | > the setting threshold*, the current channel temperature offset error out-of-bounds event occurs. The general setting is $1\%*2^{15}$.	RW	0x147

7.3.2.1.12.ECT_PROTECT_UGAIN register (0xDC)

Address: DCH; Word length: 4 bytes; Default: 0x147.

Bit(s)	Name	Description	R/W	Reset
31:16	Reserved	Reserved	RO	0
15:0	ECT_PROTECT_UGAIN	Voltage channel (UA/UB/UC) automatic temperature offset error protection threshold setting. When | t*he current channel gain factor (ECT_ UxGAIN register) offset by the voltage channel | > the setting threshold*, the temperature compensation error of the current channel is out of bounds. The general setting is 1%*2^15.	RW	0x147

7.3.2.1.13. ECT_PROTECT_INGAIN register (0xDD)

Address: DDH; Word length: 4 bytes; Default:0x147;

Bit(s)	Name	Description	R/W	Reset
31:16	Reserved	Reserved	RO	0
15:0	ECT_PROTECT_INGAIN	IN-channel automatic temperature offset error protection threshold setting. When | *the voltage channel gain factor (ECT_ INGAIN register) offset by the IN channel | > the setting threshold*, the IN-channel temperature-compensated error out-of-bounds event occurs. The general setting is 2%*2^15.	RW	0x147

7.3.2.1.14. ECT_LT_Kxx register (0xDE~0xE4)

The Low temperature segment Ix channel error temperature offset linear fitting coefficient register

Address: DEH~E0H; Word length: 4 bytes; Default:0x0;

Bit(s)	Name	Description	R/W	Reset
31:17	Reserved	Reserved	RO	0
16:0	ECT_LT_KIx	The temperature offset linear fitting coefficient of the Ix channel error in the low temperature segment LT_KIx (x=A,B,C) register. According to the low temperature segment characteristics of the Ix channel measured by the user in the calibration stage, the value is calculated and written to EEPROM for storage, and the MCU writes the register when powering on. After the current channel gain is calibrated, the nominal current temperature curve of -40°C~25°C is scanned, and the most suitable linear fitting temperature point T', the	RW	0

measured current is Ix (25) at 25°C, and the current Ix (T') of the fitting temperature T'; If the temperature curve of the entire low temperature segment is the smallest distance from the line spacing formed by connecting Ix(25) and Ix(T'), the calculation formula of LT_KIx is LT_KIx=ERR/ (T'-25), ERR= (Ix (T')-Ix(25)) /Ix (25)

The highest bit is the sign bit, the total-scale range is 0.022, and the default is 0

The temperature offset linear fitting coefficient of Ux channel error in the low temperature segment register

Address: E1H~E3H; Word length: 4 bytes; Default:0x0;

Bit(s)	Name	Description	R/W	Reset
31:17	Reserved	Reserved	RO	0
16:0	ECT_LT_KUx	The temperature compensated linear fitting coefficient of the Ux channel error in the low temperature segment LT_Kux register. According to the low temperature segment characteristics of the Ux channel measured by the user in the calibration stage, this value is calculated and written to EEPROM for storage, and when power-on, the MCU exports and writes to the register from EEPROM. After the voltage channel gain is corrected, the nominal voltage and temperature curve of -40°C~25°C is scanned, and the most suitable linear fitting temperature point T', the measured voltage of 25°C is Ux (25), and the voltage of the fitting temperature T' is Ux (T'); If the temperature curve of the entire low temperature segment is separated from Ux(25) and Ux(T') to form a minimum linear spacing, the calculation formula of LT_KUx is LT_KUx=ERR/ (T'-25), ERR= (Ux (T')-Ux(25)) /Ux (25) The highest bit is the sign bit, the total-scale range is 0.022, and the default is 0	RW	0

The temperature offset linear fitting coefficient of the IN channel error in the low temperature segment register

Address: E4H; Word length: 4 bytes; Default: 0x0;

Bit(s)	Name	Description	R/W	Reset
31:17	Reserved	Reserved	RO	0
16:0	ECT_LT_KIN	The error temperature offset linear fitting coefficient of the IN channel in the low temperature segment LT_KIN register. According to the low temperature segment characteristics of the IN channel measured by the user in the calibration stage, this value is calculated and written to EEPROM for storage, and the register is written by the MCU when powering up.	RW	0

		After the gain calibration of the IN channel, the nominal current temperature curve of -40°C~25°C was scanned, and the most suitable linear fitting temperature point T', the measured current of 25°C was IN (25) and the current of the fitting temperature T' was IN (T'); If the temperature curve of the entire low temperature section is the smallest distance between the straight lines connected by IN(25) and IN(T'), the calculation formula of KIN is LT_KIN=ERR/ (T'-25), ERR=(IN(t')-in(25)) /IN (25) The highest bit is the sign bit, the total-scale range is 0.022, and the default is 0		

7.3.2.1.15. ECT_HT_Kxx register (0xE5~0xEB)

The temperature offset linear fitting coefficient of the Ix channel error in the high temperature segment registers

Address: E5H~E7H; Word length: 4 bytes; Default: 0x0;

Bit(s)	Name	Description	R/W	Reset
31:17	Reserved	Reserved	RO	0
16:0	ECT_HT_KIx	The error temperature offset linear fitting coefficient of the IN channel in the low temperature segment LT_KIN register. According to the low temperature segment characteristics of the IN channel measured by the user in the calibration stage, this value is calculated and written to EEPROM for storage, and the register is written by the MCU when powering up. After the gain calibration of the IN channel, the nominal current temperature curve of -40°C~25°C was scanned, and the most suitable linear fitting temperature point T', the measured current of 25°C was IN (25) and the current of the fitting temperature T' was IN (T'); If the temperature curve of the entire low temperature section is separated from IN(25) and IN(T') to form a minimum linear spacing, the calculation formula of KIN is LT_KIN=ERR/ (T'-25), ERR=(IN(t')-in(25)) /IN (25) The highest bit is the sign bit, and the default is 0	RW	0

The temperature offset linear fitting coefficient of the Ux channel error in the high temperature section registers

Address: E8H~EAH; Word length: 4 bytes; Default: 0x0;

Bit(s)	Name	Description	R/W	Reset
31:17	Reserved	Reserved	RO	0

Bit(s)	Name	Description	R/W	Reset
16:0	ECT_HT_KUx	The temperature offset linear fitting coefficient of Ux channel error in the high temperature section HT_Kux register. According to the high-temperature segment characteristics of the Ux channel measured by the user in the calibration stage, the value is calculated and written to EEPROM for storage, and when power-on, the MCU exports and writes to the register from EEPROM. After the voltage channel gain is calibrated, the nominal voltage and temperature curve of -40°C~25°C is scanned, and the most suitable linear fitting temperature point T', the measured voltage of 25°C is Ux (25), and the voltage of the fitting temperature T' is Ux (T'); If the temperature curve of the entire high temperature segment is the smallest distance between the straight lines connected by Ux(25) and Ux(T'), the calculation formula of HT_KUx is HT_KUx=ERR/ (T'-25), ERR= (Ux (T')-Ux(25)) /Ux (25) The highest bit is the sign bit, and the default is 0	RW	0

The temperature offset linear fitting coefficient of IN channel error in the high temperature section registers

Address: EBH; Word length: 4 bytes; Default: 0x0;

Bit(s)	Name	Description	R/W	Reset
31:17	Reserved	Reserved	RO	0
16:0	ECT_HT_KIN	The temperature offset linear fitting coefficient of the IN channel error in the high temperature segment HT_KIN register. According to the high temperature segment characteristics of the IN channel measured by the user in the calibration stage, this value is calculated and written to EEPROM for storage, and the register is written by the MCU when power-on. After the gain calibration of the IN channel, the nominal current temperature curve of -40°C~25°C was scanned, and the most suitable linear fitting temperature point T', the measured current of 25°C was IN (25) and the current of the fitting temperature T' was IN (T'); If the temperature curve of the entire high temperature section is the smallest distance from the line formed by connecting IN(25) and IN(T'), the calculation formula of KIN	RW	0

| | | HT_KIN=ERR/ (T'-25), ERR=(IN(t')-in(25)) /IN (25) The highest bit is the sign bit, and the default is 0 | | |

7.3.2.1.16.ECT_TEMP register (0xEC)

Address: ECH; Word length: 4 bytes; Default: 0x0;

Bit(s)	Name	Description	R/W	Reset
31:10	Reserved	Reserved	RO	0
9:0	ECT_TEMP	The register of single and cyclic automatic temperature offset mode: the register saves the temperature value of this automatic temperature offset detection : TEMP+TEMPOS, regardless of whether this temperature offset meets the conditions of adjusting the offset coefficient register, the temperature value of this detection is written into the register; Semi-automatic mode: the register saves the external temperature measurement and manually writes the temperature value to start the hardware temperature offset (ECT_CMD_STA. CMD_STA Enable) and the hardware takes this temperature value as input. Manual mode: Clear the register.	RW	0

7.3.2.1.17. ECT_RESULT_WREN register (0xED)

Address: EDH; Word length: 4 bytes; Default: 0x0;

Bit(s)	Name	Description	R/W	Reset
31:6	Reserved	Reserved	RO	0
5:0	ECT_RESULT_WREN	=0xEA, EEH-F5H error temperature offset results register ECT _IxGAIN, ECT _UxGAIN, ECT _INGAIN, ECT_TEMP_UD write enabled. =0x0, these registers are write-protected to write other values, which are invalid	RW	0

7.3.2.1.18. ECT_xxGAIN register (0xEE~0xF4)

Current channel error temperature offset gain register

Address: EEH~F0H; Word length: 4 bytes; Default: 0x0;

Bit(s)	Name	Description	R/W	Res

					et
31:16	Reserved	Reserved		RO	0
15:0	ECT_ IxGAIN	The temperature offset gain factor of the Ix channel is located after the Ix channel gain calibration register of the EMU block. Manual mode, turned on ECT_RESULT_WREN write protection and configured by the software; Automatic temperature offset mode: When the temperature offset condition is met, it is automatically written by the automatic temperature offset unit. Calculation formula (take the low temperature segment as an example): $ECT\_IxGAIN = -LT\_KIx*(T-25)/(1+LT\_KIx*(T-25))$, where LT_KIx is the automatic temperature offset linear fitting coefficient of the Ix channel error in the low temperature segment, see the ECT_LT_KIx register description for details; T is the temperature measurement value of this compensation. The high temperature segment uses the high temperature segment offset the K factor ECT_HT_KIx, and the formula is the same as above. Whether to use the high temperature segment or low temperature segment for calculation is automatically determined by the hardware The highest bit is the sign bit, the total-scale range is 1, and the default is 0		RW	0

Voltage channel error, temperature offset, gain register

Address: F1H~F3H; Word length: 4 bytes; Default: 0x0;

Bit(s)	Name	Description	R/W	Reset
31:16	Reserved	Reserved	RO	0
15:0	ECT_ UxGAIN	Temperature offset gain factor for the UX channel. Manual mode is configured by the software after turned on the write protection of ECT_RESULT_WREN; Automatic temperature offset mode: When the temperature offset condition is met, it is automatically written by the automatic temperature offset unit. Calculation formula (take the low temperature segment as an example): $ECT\_UxGAIN = -LT\_KUx*(T-25)/(1+LT\_KUx*(T-$	RW	0

25)),

where LT_KUx is the automatic temperature offset linear fitting coefficient of Ux channel error in the low temperature segment, see ECT_LT_KUx register description for details; T is the temperature measurement value of this offset.

The high temperature segment uses the high temperature segment to offset for the K-coefficient ECT_HT_KUx, and the formula is the same as above.

Whether the calculation is automatically judged by the hardware using the high temperature segment or the low temperature segmentn.

The highest bit is the sign bit, the total-scale is 1, and the default is 0

IN channel error temperature offset gain register

Address: F4H; Word length: 4 bytes; Default: 0x0;

Bit(s)	Name	Description	R/W	Reset
31:16	Reserved	Reserved	RO	0
15:0	ECT_ INGAIN	Temperature offset gain factor for the IN channel. Manual mode is configured by the software after turned on the write protection of ECT_RESULT_WREN; Automatic temperature offset mode: When the temperature offset condition is met, it is automatically written by the automatic temperature offset unit. Calculation formula (take the low temperature section as an example): ECT _INGAIN=-LT_KIN* (T-25)/(1+LT_IN*(T-25)), where LT_KIN is the automatic temperature offset linear fitting coefficient of Ux channel error in the low temperature segment, see the description of ECT_LT_KIN register for details; , T is the temperature measurement value of this offset. The high temperature segment uses the high temperature segment to offset for the K-factor ECT_HT_KIN, and the formula is the same as above. Whether the calculation using the high temperature segment or the low temperature segment is automatically determined by the hardware. The highest bit is the sign bit, the total scale is 1, and the default is 0	RW	0

7.3.2.1.19. ECT_TEMP_UD register (0xF5)

Address: F5H; Word length: 4 bytes; Default: 0x64;

Bit(s)	Name	Description	R/W	Reset
31:10	Reserved	Reserved	RO	0
9:0	ECT_TEMP_UD	The register holds the temperature values detected by the most recently updated temperature offset factor register group (ECT_IxGAIN, ECT_UxGAIN, ECT_INGAIN) SARADC detection. Single-time and cyclic automatic temperature offset mode and semi-automatic temperature offset mode are automatically written by ECT after updating the temperature offset coefficient register group. Manual mode, the register is filled in by the software.	RW	0x64

7.3.2.1.20. SARADC_TADJ register (0xF6)

Address: F6H; Word length: 4 bytes; Default: 0x0683_0111;

Bit(s)	Name	Description	R/W	Reset
31:27	Reserved	Reserved	RO	0
26:16	TADJ	Single-point calibration value for mass production temperature, the recommended value is 0x699_4311	RW	0x683_0111

7.3.2.1.21.SARADC_TEMP register (0xF7)

Address: F7H; Word length: 4 bytes;

Bit(s)	Name	Description	R/W	Reset
31:11	Reserved	Reserved	RO	0x0
10	Temp_valid	SARADC temperature measurement output temperature value TEMP_OUT valid state, 0 is invalid, and 1 output temperature value is valid	RO	0x0
9:0	TEMP_OUT	SARADC measure the current temperature value. Two's complement means that 10 significant bits, BIT9 is the sign bit; The minimum scale is 0.25°. The conversion formula to the actual temperature is T=TEMP_OUT/4, indicating that the range is -128°~+127.75° Note that manually start SARADC temperature measurement, that is, write 1 to SAR_CTL1.kick register bit, ECT hardware temperature offset is recommended not to be enabled to prevent signal	RO	0x0

		conflicts.		

7.3.2.1.22.SAR_EN register (0xF8)

Address: F8H; Word length: 1 bytes; Default:0;

Bit(s)	Name	Description	R/W	Reset
7:1	Reserved	Reserved	RO	0x0
0	EN	SARADC module enable signal = 1，SARADC module enable; = 0，SARADC module disable.	RW	0