Single-phase metering chip MKE101R users manual

Rev 1.0

Version Update Notice

version number	Modification time	revise content
Rev 1.0	2025-02-13	First release

catalogue

1 Chip Introduction

The MKE101R, a high-precision and highly reliable single-phase metering chip by MAKSA, is designed for various metering applications including smart meters, energy consumption analysis, power monitoring, and electrical safety.

1.1 Chip Characteristics

- ✓ calculate
  - It provides a three-channel sum-delta ADC, including the voltage channel (U channel), current channel A (IA channel), and current channel B (IB channel).①
  - The IA channel PGA supports 4x,8x,12x,16x (default), 24x, and 32x amplification, but not 1x or 2x. The IB and U channel PGA support 1x,2x, and 4x amplification.②
  - The active power metering performance of the front line (A line) shows a nonlinear error of <0.1% within a dynamic range of 20000:1.③
  - The reactive power metering performance of the line maintains a non-linear error below 0.1% within a dynamic range of 20000:1.
  - It provides three-channel RMS measurement. The IA channel has a dynamic range of 2000:1 with a nonlinearity error <0.1%. The IB and U channels have a dynamic range of 1000:1 with a nonlinearity error <0.1%.
  - Provides two-phase active and reactive power output on the live and neutral lines (B channel), supporting dual-phase active and reactive power metering.
  - A pulse frequency generator is provided for accumulating and integrating electrical energy at user-defined power levels.
  - Provide three-channel ADC instantaneous sampling values and support instantaneous sampling value update interrupts
  - The threshold for latent movement can be adjusted.
  - It provides reverse active power indication and outputs the REVP reverse indication signal through the QF pin.
  - Provide U-channel frequency measurement
  - Provide U-channel zero-crossing detection
  - Supports zero-crossing signals from Ia channels to be output through the TX pin of the UART port.
  - Supports reference voltage monitoring, see VREF_OK
  - Supports bidirectional measurement to meet the requirements for rapid power flow change testing
  - Active power supports both full-wave and fundamental wave metering.
  - reactive power support fundamental wave metering
  - Both active and reactive power support half-wave metering
- ✓ software calibration
  - The meter constant (HFConst) is adjustable.
  - Provide gain and phase correction

- Provide active, reactive, and RMS offset correction
- Provide small signal calibration acceleration function
- Enable automatic configuration parameter validation

✓ Supports arbitrary single-channel, dual-channel, or triple-channel ADC waveform buffering, with continuous waveform acquisition via SPI/UART ports.

✓ The RX input pin of a UART module serves dual functions: global reset (via the pin) and local reset (via the UART module).

✓ Features power monitoring capability

✓ Electric energy register with timing freeze function

✓ Supports synchronous sampling

✓ Supports fast leakage detection

✓ Supports DC detection

✓ Supports voltage and current transient event detection

✓ Supports single-phase three-wire ±P1±P2 and ±Q1±Q2 integration operations

✓ Configure register support for CRC16

✓ Supports adjustable pulse width and level inversion for power

✓ Supports Ia±Ib RMS calculation

✓ Supports asymmetric baud rate UART communication. The TX module features HSTX functionality with a baud rate of Fosc/4 (crystal oscillator frequency). HSTS automatically transmits real-time waveforms, metering parameters, power pulses, interrupts, and other data. The RX baud rate and communication parameters remain unchanged.

✓ Supports IIC host communication for convenient interaction with external temperature sensor chips, used for terminal temperature measurement.

✓ Supports error self-monitoring function

✓ Supports software-adjustable UART baud rate

✓ The MKE101R operates on a +5V/3.3V power supply, with typical power consumption values of

Crystal frequency / Power supply voltage	5V	3.3V
3.579545MHz	2 7mW	15mW
5.5296MHz	30 mW	16 mW

✓ Built-in 1.25V±1% reference voltage, with a typical temperature coefficient of 5ppm/℃ and a maximum of 15ppm/℃.

✓ The MKE101R is packaged in SOP16L green packaging.

① Channel A is called IA channel, channel B is called IB channel, and channel U is called U channel.
② In this article, red text indicates new or upgraded features in V5, which will not be repeated later.
③ The live wire is called A line, and the neutral wire is called B line.

1.2 Function Overview

The MKE101R meter provides comprehensive measurement capabilities for all-wave and fundamental wave active/reactive power, voltage/current RMS values, line frequency, and half-cycle updates of active/reactive power and voltage/current values. It supports dual independent channels for active/reactive power and current RMS values, with full compliance to all current metrology standards including active energy metering, reactive energy metering, fundamental wave metering,

half-wave metering, and bidirectional metering.

The MKE101R features fully digital gain, phase, and offset calibration. Active power pulses are output from the PF/QF/IRQ pins, while reactive power pulses, user-defined power pulses, and REVP can be output from the same pins.

The MKE101R features both SPI and UART serial interfaces, enabling seamless communication with external microcontrollers.

The MKE101R features an IIC host interface for seamless communication with external temperature sensor chips, enabling terminal temperature measurement.

The MKE101R features an HSTX interface (high-speed UART TX interface) that automatically transmits real-time waveforms, measurement parameters, pulses, and other data.

The power monitoring circuit inside MKE101R can ensure the reliable operation of the chip when power is on and off.

1.3 Function Block Diagram

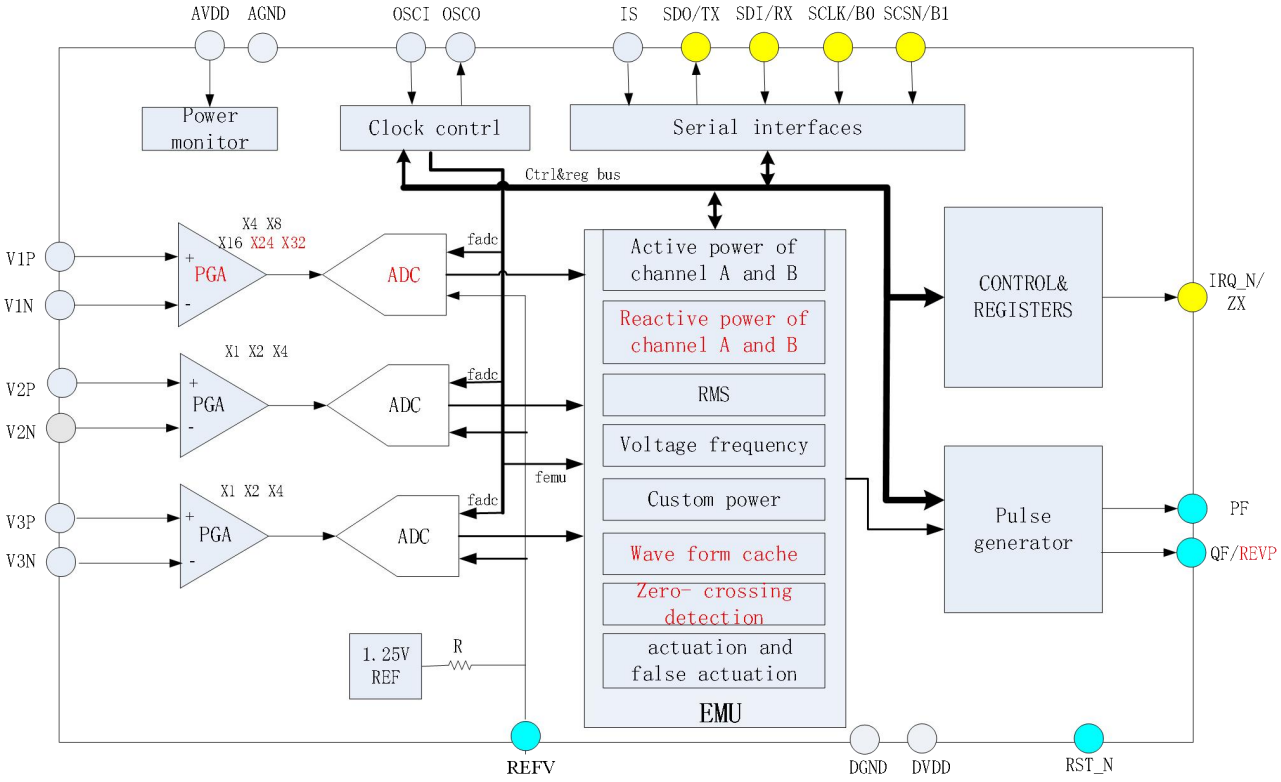


Figure 1-1 Function Block Diagram

1.4 Pin Definitions

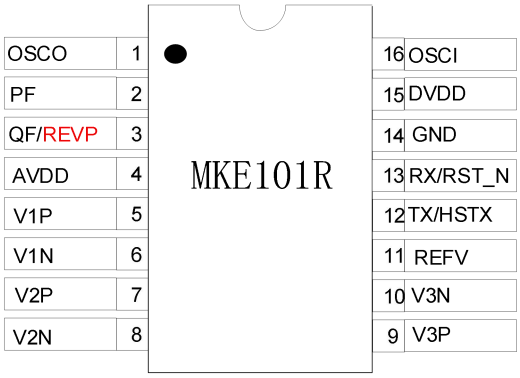


Figure 1-2 Pin layout diagram of MKE101R-SOP16L

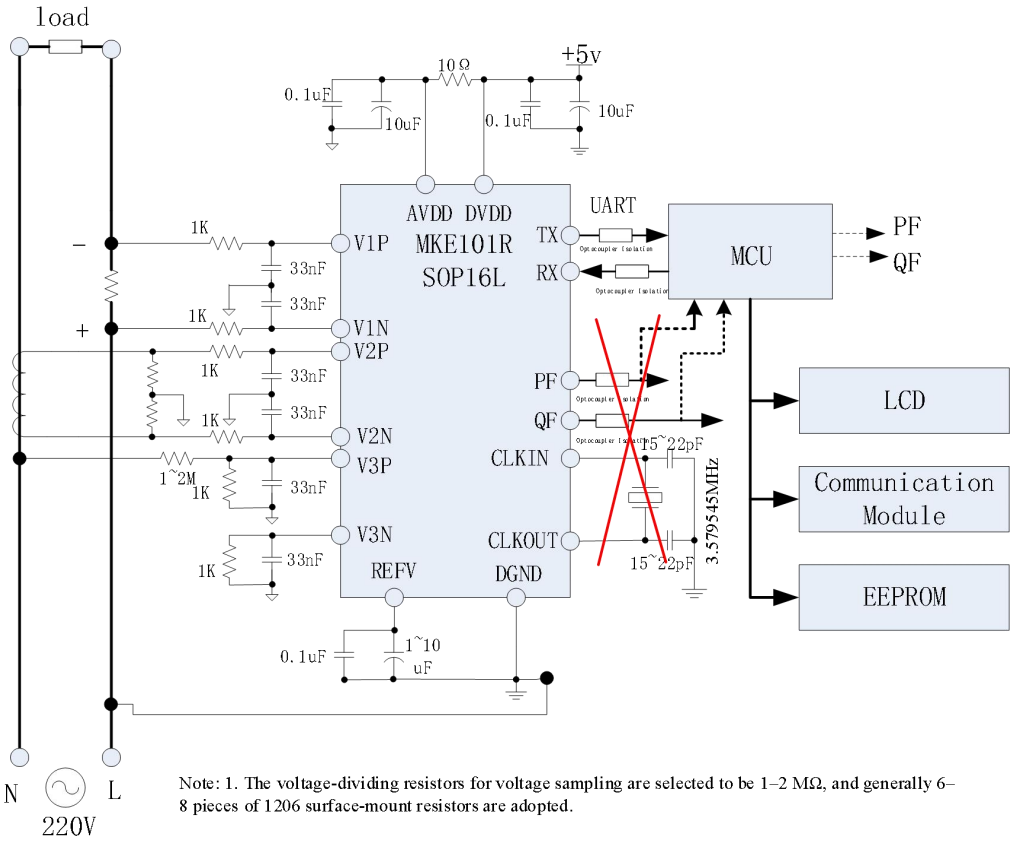
pin	characteristic	characteristic	functional description
1	OSCO	output	The output of the external crystal.
2	PF	output	The active power pulse output defaults to low-level output. Its frequency reflects the instantaneous active power level. It has a 5mA output and current absorption capability.
3	QF/ REVP	output	This pin is a QF/REVP multiplex pin (default QF). When EMUCON2.QFCFG=0, it functions as a QF pin to output either reactive power verification pulses or user-defined pulses, with low-level output as the default. The frequency reflects the magnitude of either reactive power or user-defined power values, which include three options: second active power, sum of two active power vectors, or user-defined power register. It features a 5mA output and current absorption capability. When EMUCON2.QFCFG=1, the REVP pin functions as a negative power indicator.
4	AVDD	source	Analog power pin. This pin supplies power to the analog section of the chip. It should be externally connected with a 10μF capacitor in parallel and a 0.1μF decoupling capacitor. Typical operating voltage range: 2.97V to 5.5V. After selecting a standard supply voltage (e.g., 5V or 3.3V), ensure the power supply fluctuation remains within ±10% of the specified range.
5，6	V1P, V1N	import	The positive and negative analog input pins of the I/O channel. It operates in full differential mode, with a maximum input voltage of ±1000mV and a maximum withstand voltage of ±6V. The external sampling circuit, when performing standard full-wave measurement, requires an anti-aliasing resistance of 1kΩ and an anti-aliasing capacitance ranging from 10nF to 33nF. For harmonic measurement or power quality analysis, the required anti-aliasing resistance is 1kΩ and the anti-aliasing capacitance is 3.3nF.

7，8	V2P, V2N	import	The positive and negative analog input pins of the IB channel. It operates in full differential mode, with a maximum input Vpp of ±1000mV and a maximum withstand voltage of ±6V. The external sampling circuit, when performing standard full-wave measurement, requires an anti-aliasing resistance of 1kΩ and an anti-aliasing capacitance ranging from 10nF to 33nF. For harmonic measurement or power quality analysis, the required anti-aliasing resistance is 1kΩ and the anti-aliasing capacitance is 3.3nF.
9，10	V3P,V3N	import	The U-channel features positive and negative analog input pins. It operates in fully differential mode, with a maximum input voltage of ±1000mV and a maximum withstand voltage of ±6V under normal operation. The external sampling circuit, when performing standard full-wave measurement, requires an anti-aliasing resistance of 1kΩ and an anti-aliasing capacitance ranging from 10nF to 33nF. For harmonic measurement or power quality analysis, the required anti-aliasing resistance is 1kΩ and the anti-aliasing capacitance is 3.3nF.
11	REFV	Input/Output	The input/output pin for the 1.25V reference voltage. The external reference source can be directly connected to this pin. Whether using an internal or external reference source, this pin should be decoupled with a minimum of 1μF capacitor in parallel with a 0.1μF capacitor.
12	TX	output	This pin serves as the TX data output port for UART. Using special commands, it can generate a zero-crossing signal for the IA channel, typically a 10ms square wave. For details, refer to the Special Commands section. The TX function can be reconfigured as HSTX. Operating at baud rates of Fosc/4 (895K@3.579545MHz or 1382K@5.5296MHz), the TX pin automatically transmits real-time waveforms, measurement parameters, pulses, and other data.
13	RX/RST_N	import	This pin serves as both the UART input RX and a reset pin. A local reset (UART module reset) occurs when the low-level input signal persists for between 10ms and 20ms, while a global reset (chip-wide reset) is triggered if the signal remains low for over 20ms. The internal reset circuit of MKE101R is completely independent of the UART communication circuit, and its pin reset function is identical to that of an independent pin reset.
14	GND	the earth	In the chip circuit, ensure this pin is not directly connected to ground points with high digital noise (e.g., DVDD decoupling capacitor), and maintain a sufficient distance from them.
15	DVDD	source	Digital power pin. This pin supplies power to the digital section of the chip. It should be externally connected with a 10μF capacitor in parallel and a 0.1μF decoupling capacitor. Typical operating voltage range: 2.97V to 5.5V. After selecting a standard supply voltage (e.g.,

			5V or 3.3V), ensure the power supply fluctuation remains within ±10% of the specified range.
16	OSCI	import	The input terminal of the external crystal or the clock input of the external clock system. The typical frequency of the external crystal is 3.579545 MHz. The typical value of the external capacitor is 15 pF to 22 pF, and there is already an internal bypass resistance of approximately 4 MΩ, so no external bypass resistor is required. For 3.579545 MHz, the ESR of the external crystal must be less than 120 ohms; for 5.5296 MHz, the ESR must be less than 80 ohms.

1.5 Typical Applications

1.5.1 State Grid Single-Phase 20 Version



Note: 1. The voltage-dividing resistors for voltage sampling are selected to be 1–2 MΩ, and generally 6–8 pieces of 1206 surface-mount resistors are adopted.

Figure 1-5 Typical Applications of State Grid Single-phase Meters

The MKE101R features three Σ - Δ ADC channels. The IA channel ADC (V1P/V1N inputs)

uses live-wire manganized copper for sampling, while the IB channel ADC (V2P/V2N inputs) employs neutral-wire transformer sampling. The U channel ADC (V3P/V3N inputs) handles voltage sampling. The high-performance IA channel ADC has a small manganized copper input signal and defaults to 16x PGA, whereas the IB and U channel ADCs have larger input signals and are configured at 1x PGA by default.

2 System Functions

2.1 Power Monitoring

The MKE101R chip incorporates a power monitoring circuit that continuously tracks the analog power supply (AVDD). The chip resets when the voltage drops below 2.6V ± 0.1V, and operates normally when the voltage exceeds 2.8V±0.1V.

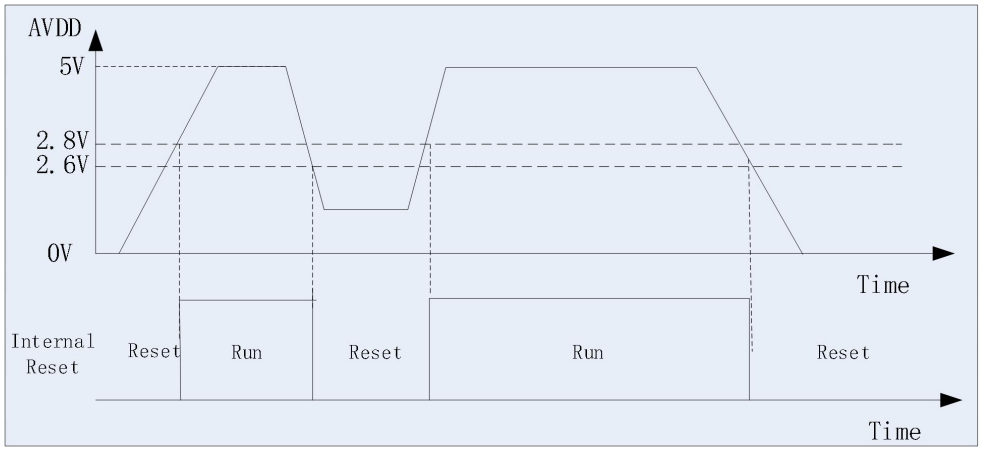


Figure 2-1 Power Supply Detection Characteristics

Normal operating range: 2.97V-5.5V. After selecting a typical supply voltage (e.g., 5.0V or 3.3V), ensure the power supply fluctuation remains within ±10% of the specified range.

2.2 System Reset

The MKE101R supports three global reset modes:

- Up and down electricity
- External pin reset or RX pin reset
- command reset

The MKE101R supports a local reset mode:

- UART module reset

➢**global reset**

When any global reset occurs, the register returns to its initial value, and the external pin levels revert to their original states.

The chip completes reset 15 microseconds after the reset command is issued.

The external reset pin of MKE101R first drops from high to low level and remains at low level for over 50 microseconds, then rises from low to high level for over 300 microseconds before releasing the reset.

The RX pin of the MKE101R also functions as a reset pin. When the input signal remains low for over 20ms at 3.579545MHz or 1 3 ms at 5.5296MHz, the metering chip recognizes this as a valid reset. This feature reduces the number of optocouplers required in isolated applications. The

internal reset circuit of the MKE101R is completely independent of the UART communication circuit, and its pin reset function is equivalent to that of an independent pin reset.

The recommended RX pin reset procedure is: first set the RX pin low for 25ms at 3.579545MHz (F osc) and 17ms at 5.5296MHz (F osc), then set it high for 20ms, and finally initiate normal UART communication.

➢**local reduction**

The RX pin of MKE101R supports UART communication port reset functionality. When the input signal on the RX pin remains low for over 10ms at 3.579545MHz or 6.5ms at 5.5296MHz, the UART communication module of the metering chip will reset.

This function is recommended only when the MCU detects UART communication anomalies. For isolated UART interface reset, the RX pin should maintain low level for 15ms at 3.579545MHz Fosc and 10ms at 5.5296MHz Fosc. Note that exceeding 20ms at 3.579545MHz Fosc or 1 3 ms at 5.5296MHz Fosc will trigger a full chip reset.

➢**Related registers:**

The RST in the system status register is a hardware reset flag: it is set to 1 when the external RST_N pin or power-up reset is completed, and cleared upon readout. This flag can be used for resetting and recalibrating data requests.

The SOFTRST in the system status register is a command reset flag: it is set to 1 when the command reset is completed and cleared after reading. This flag can be used for resetting and requesting calibration data.

It is suggested that the CPU should reset the metering chip by pin reset or command reset before initializing the metering chip.

2.3 Module Conversion

The MKE101R features three ADC channels: IA for live wire current sampling, IB for neutral wire current sampling, and U for voltage sampling. The SYSCON register (SYSCON 0x00H) with SYSCON[6] enables or disables the IB channel.

The ADC employs full-differential input, with the maximum signal input amplitude for current and voltage channels reaching 1000mVpp at peak.

By configuring SYSCON[5:0] in the SYSCON register and SYSCON2[1:0] in System Control Register 2 (SYSCON2 0x19H), the PGA of three ADC channels can be set individually. The IA channel PGA options are 4, 8, 12,16 (default), 24, or 32; while the IB and U channel PGA options are 1 (default), 2, or 4.

2.4 Active Power

The MKE101R provides dual active power calculation and correction channels: A and B. The power update frequency is Fosc/2/2^19 (default), with 3.414Hz at Fosc 3.579545MHz and 5.27Hz at Fosc 5.5296MHz. Other update frequencies are configurable, as detailed in EMUCON2.UPMODE.

The register also contains two sets of registers for phase correction, active offset correction, active gain correction, and average power. The IB channel includes the gain correction register IBGain, which affects the active power of the B channel and the IB RMS value.

The current average active power (PowerP) channel for detecting latent motion and activation,

along with the instantaneous active power channel (DATAP) for calculating active energy, are selected between channels A and B based on specific commands, as detailed in the Special Commands section.

The user can configure the channel selection through special commands, and the configuration results can be queried via the CHNSEL register bit.

The digital high-pass filter in Figure 2-2 is mainly used to remove the DC component in the current and voltage sampling data.

In Figure 2-2, DCIA, DCIB, and DCU are used to correct the DC bias of the ADC channel. When the MKE101R is used for DC measurement applications, it is necessary to correct the DC bias and disable the high-pass filter.

2.5 Reactive Power

The MKE101R features dual reactive power and reactive energy calculation circuits for PowerQ/PowerQB and dual reactive energy. The power update frequency is set to Fosc/2/2^19 (default), with 3.414Hz@Fosc3.579545MHz and 5.27Hz@Fosc 5.5296MHz. Other update frequencies are configurable, as detailed in EMUCON2.UPMODE.

The MKE101R features dual-channel fundamental reactive power and electrical energy calculation. As the fundamental reactive power function cannot support two channels simultaneously, it defaults to outputting A-channel fundamental reactive power. A dedicated command allows switching to B-channel fundamental reactive power output.

2.6 Effective Value

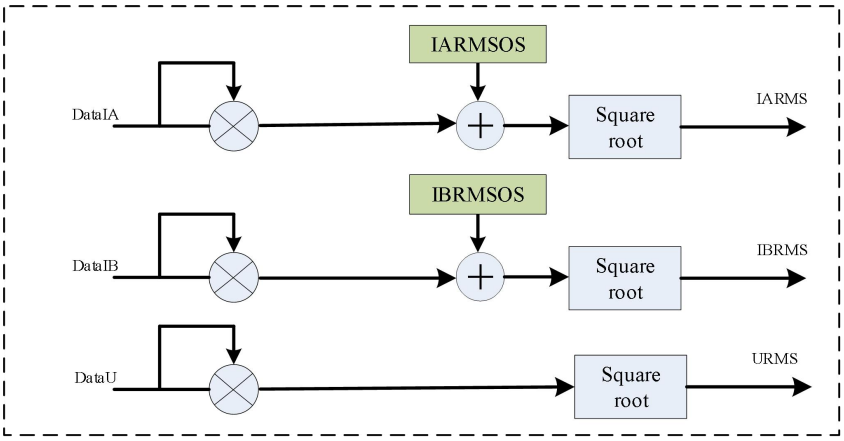


Figure 2-4 Effective Value Calculation Block Diagram

The MKE101R provides three-channel true RMS output parameters: URMS, IARMS, and IBRMS. With a 24-bit word length, it supports true RMS updates at three frequencies: 3.414Hz at 3.579545MHz Fosc (default), 5.27Hz at 5.5296MHz Fosc, and customizable frequencies as specified in EMUCON2.UPMODE. The device also includes two true RMS offset registers: IARMSOS and IBRMSOS.

Channel 2 gain correction (IBGain) affects the output of IBRMS, while other phase corrections, power gain corrections, and power offset corrections do not affect the RMS calculation results.

2.7 Energy Calculation

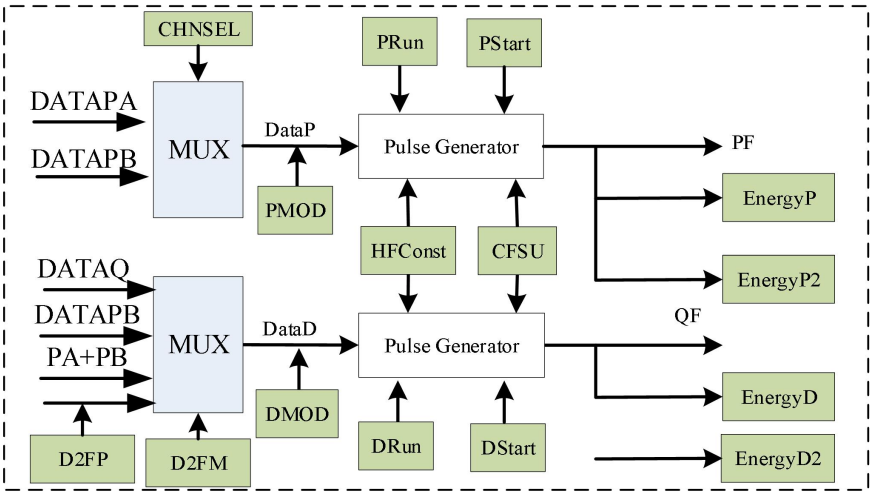


Figure 2-5 Energy Calculation

Energy pulse output:

THE PULSE OUTPUT, ALSO KNOWN AS CALIBRATION PULSE OUTPUT, CAN BE DIRECTLY CONNECTED TO A STANDARD ELECTRICITY METER FOR ERROR COMPARISON.

THE PF/QF OUTPUT MUST SATISFY THE FOLLOWING TIMING RELATIONSHIP:

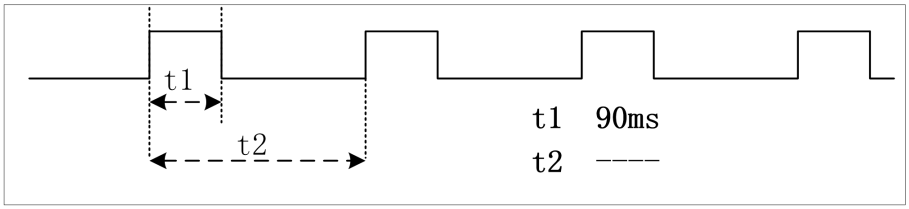


Figure 2-6 Output Pulse Width

Note: When the pulse output period is less than 180ms, the pulse is output in equal duty form.

Relationship between PFcnt/DFcnt, HFConst, pulse output, and energy register:

When 2*|PFcnt| (0x20H) equals HFConst (0x02H), the PF generates a pulse output. Simultaneously, the energy registers EnergyP (0x29H) and EnergyP2 (0x2AH) are incremented by 1.

When 2*|DFcnt| (0x21H) equals HFConst (0x02H), the QF generates a pulse output. Simultaneously, the energy registers EnergyD (0x2BH) and EnergyD2 (0x2CH) are incremented by 1.

Relationship between pulse output, energy register, and PRun/DRun and PStart/DStart:

The active / custom energy register and PF / QF output are also controlled by PRun / DRun and PStart / DStart.

- When PRun equals zero or |P| is less than PStart, the PF does not generate pulses, and neither PFcnt nor the functional quantity register increments.
- When DRun equals zero or |DataD| is less than DStart, the QF does not generate pulses, and neither DFcnt nor the custom energy register increments.

Custom pulse output:

DataDs default source is DATAQ (reactive power), but users can select DATAPB (second active power channel), DATAPA+DATAPB (two-channel power vector sum), or D2FP (user-defined) through the D2FM register to specify the power source.

Pulse output acceleration:

To accelerate small-signal correction, the system provides pulse output acceleration capability. During correction, the CFSUEN and CFSU[1:0] bits of the EMUCON (0x01H) register can be configured to boost the output frequency of PF/QF, achieving up to 16-fold enhancement.

Reverse direction:

When the active or custom power is negative, the REVP or REVQ bit in the EMUStatus register is set to 1. The REVP bit updates in sync with the PF pulse, while the REVQ bit updates in sync with the QF pulse.

2.8 Channel Switching

The MKE101R features a dedicated ADC channel for zero-line current RMS and power measurement, with A/B channel switching capability to enable users to select specific current channels for active power measurement.

Channel switching is implemented via special command words (see Special Command Registers section). The configuration results can be queried through the CHNSEL register bit.

2.9 Frequency Measurement

The MKE101R directly outputs line frequency parameters (UFreq 0x25H) to measure fundamental frequency. Its minimum measurement frequency is 6.8Hz at 3.579545MHz frequency, and 4.4Hz at 5.5296MHz frequency, with a measurement bandwidth of 250Hz.

The MKE101R also features an additional line frequency parameter register (UFreq2 0x35) for measuring fundamental frequency, with a minimum measurement frequency of 1Hz at 3.579545MHz and 0.65Hz at 5.5296MHz, and a measurement bandwidth of 250Hz.

2.10 Start-up of the Submerged Motor

The start threshold is configured by the PStart and DStart registers. These 16-bit unsigned numbers are compared with the absolute values of the high 24 bits of PowerP and DataD (32-bit signed numbers) to determine the start condition.

When PowerP is less than PStart, PF does not output pulses.

When DataD is less than DStart, QF does not output pulses.

The default reset value for PStart is 0x0060H, and for DStart, it is 0x0120H.

When the power is below the startup power, the NoPld bit in the EMUStatus register is set to 1; when the active power reaches or exceeds the startup power, the NoPld bit is cleared to 0.

When DataD is below the startup power, NoPld is set to 1; when the custom power reaches or exceeds the startup power, NoPld is reset to 0.

2.11 Event Detection

The MKE101R enables/disables zero-crossing output via the ZXCFG (EMUCON.7) configuration, using the IRQ_N/ZX pin.

The MKE101R supports four zero-crossing output modes by configuring the ZXD1 (EMUCON.9) and ZXD0 (EMUCON.8) register bits.

The MKE101R supports the UART TX pin to output an IA zero-crossing signal. In UART communication mode, a special command can be set to enable the TX pin to output an IA zero-crossing signal, typically a 10ms square wave. If the channel special command or the UART RX pin remains low for over 10ms, the UART module will reset and disable the zero-crossing output function, reverting to the TX function of the UART communication port. For details, refer to the special commands section.

The MKE101R supports voltage and current event detection, including voltage drop, overload in current channel A, overload in current channel B, and overload in voltage channel.

The event threshold register includes: voltage drop threshold register USAG, current channel A peak detection threshold register, current channel B peak detection threshold register, voltage channel peak detection threshold register.

The voltage drop threshold register is a 16-bit unsigned number. This function remains disabled when the value is zero. Upon writing a non-zero value, voltage drop detection is activated. The threshold is compared with the high 16 bits of the 24-bit waveform sampling value from channel 24, with the detection half-period count determined by SYSCON2.USAG_CFG[7:0]. If the voltage drop duration exceeds the USAG_CFG threshold, a voltage drop event is triggered, and the detection result is reported as an interrupt.

The peak detection threshold register is a 16-bit unsigned number. This function remains disabled when the value is zero. Upon writing a non-zero value, the drop detection is activated. The threshold is compared with the high 16 bits of the 24-bit waveform sampling value from channel 24, which is sampled synchronously with the current. If the waveform sampling value exceeds the threshold, an overload event is triggered, and the detection result is reported via an interrupt.

Note: The 24-bit waveform sampling value of the synchronous sampling channel is approximately 0.5*Vin*2^23, where Vin is the normalized input signal value, and the normalized value is 1 when the amplitude is 1V.

2.12 Interruption

The MKE101R interrupt resources comprise: 1 interrupt enable register (IE), 2 interrupt status registers (IF and RIF), and a multiplexed interrupt request pin (IRQ_N/ZX). The RIF and IF registers function in tandem-reading RIF clears IF, and vice versa.

The MKE101R waveform buffer interrupt resources comprise two registers: WAVE_IE (waveform buffer interrupt enable) and WAVE_IF (waveform buffer status). Writing to the WAVE_IF flag clears both the flag and the associated interrupt.

1. Interrupt request signal IRQ_N

The IRQ_N/ZX pin serves as a multiplexed signal combining IRQ_N and zero-crossing detection output ZX. Its function is determined by configuring the ZXCFG bit in the EMUCON register (0x01H).

When the interrupt enable bit in the interrupt enable register is set and an interrupt occurs, the IRQ_N pin remains low. The pin returns to high when the CPU reads RIF or IF via the SPI interface, following the SCLK falling edge of the last bit (LSB) in the command byte.

2. Interrupt Handling Process

hardware ：

- The IRQ_N pin of MKE101R is typically connected to the MCUs external interrupt pin (INT). When IRQ_N transitions from high to low, the MCU generates an INT interrupt.
- The MCU acts as the host for SPI or UART, while the MKE101R functions as the slave for SPI or UART.

interrupt handler ：

Step 1: MCU Interrupt Initialization

1. The MCU reads the MKE101R RIF and clears the interrupt flags for IF and RIF;
2. Configure the MKE101R IE register to enable the required interrupt enable bit for generating IRQ_N;
3. Enable the MCUs INT external interrupt, wait for the MKE101R interrupt event to occur, then the IRQ_N output triggers the INT interrupt, jumping to the INT interrupt entry address.

Step 2: Interrupt Service Routine in MCU

1. Disable the MCUs global interrupt and INT interrupt;
2. The MCU reads the RIF register via SPI, clears both the IF and RIF registers, and sets IRQ_N back to high level.
3. The MCU determines the interrupt source of MKE101R by checking the RIF interrupt flag, then executes the corresponding interrupt handler.
4. After executing the interrupt handler, the MCU activates both global and INT interrupts, then returns to the original state.

After returning from an interrupt, if the /INT interrupt flag is detected, the program re-enters the external interrupt service routine (ISR) and repeats step 2. If the /INT interrupt flag is not detected, it indicates no interrupt event occurred during the interrupt handling process, and the program continues to run.

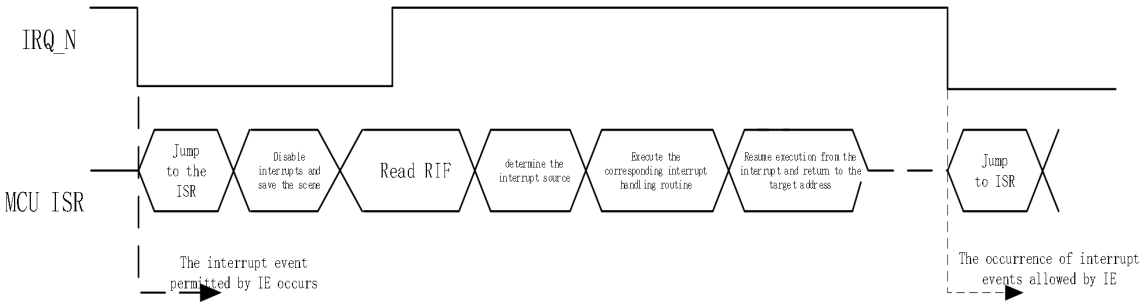


Figure 2-7 MKE101R interrupt handling process

2.13 Waveform Buffer

The MKE101R features a built-in 256 × 20-bit SRAM waveform buffer module that stores ADC sampling waveforms for FFT analysis and power quality evaluation.

The waveform buffer source supports three options: full-wave data (Fosc/2/128 sampling rate), fundamental wave data (Fosc/2/128 sampling rate), and synchronous sampling data (determined by synchronization configuration). It also allows buffering of any single, dual, or triple-channel waveform data from the IA/IB/U channels.

Users can access the cache content through various read commands. The read pointer increments by 1 for each accessed point. When the address exceeds the cache length, it resets to the starting address.

Users can change the read pointer position using special commands (configure the waveform pointer address). The read pointer automatically resets to the starting address each time the waveform buffer is started.

2.13.1 Characteristics of Waveform Buffer

- The waveform buffer has a maximum size of 256×20, with a depth of 256 addresses. Each buffer contains 20 bits of waveform data.
- The waveform buffer can be configured to use either full-wave measurement data, fundamental wave measurement data, or synchronized sampling channels as the data source.
- Supports continuous and single cache
- You can cache I1/I2/U three-channel waveform data. Each data source can be configured as single-channel, dual-channel, or three-channel cache. The three-channel cache stores 64 points per channel.
- In multi-channel caching, two caching modes can be selected: channel contiguous caching and channel cross caching.
- Configure interval caching to double or quadruple the interval
- Waveform data can be read out through three interfaces: SPI, UART, and HSTX. When reading data, you can select either 24-bit or 16-bit waveform data, and different channels can be independently selected.
- Waveform data output supports high byte first/low byte first
- The read pointer automatically returns to the first address each time the waveform buffer is initialized.
- Continuous buffering uses ping-pong operation to cache and output real-time waveforms.
- The software can read the busy flag or obtain the waveform buffer status through interrupts.
- When the cache reaches half full, the half-block SRAM waveform data can be read out via the SPI or HSTX interfaces.
- Software-readable busy flag or data overwrite interrupt, retrieve waveform buffer status

2.13.2 Waveform Buffering Method

data cache speed

The waveform buffers capacity and half-full time are shown in the table below, with 256-point waveforms loaded each time.

number of channels	intermediate buffer configure	SRAM size (dots)	Cache half-full time (ms)	Cache full time (ms)
1	4x buffer	256	40	80
2	4x buffer	256	20	40
3	4x buffer	192	10	20
1	double buffer	256	20	40
2	double buffer	256	10	20
3	double buffer	192	5	10
1	Cache all	256	10	20
2	Cache all	256	5	10
3	Cache all	192	2.5	5

Since the length of the waveform data in the cache is 20 bits, which is not a multiple of 8, it is not convenient to frame the received data. Therefore, the chip usually processes the waveform data to 24 bits or 16 bits when sending.

Data output speed

The waveform data is processed for 16-bit transmission, with its data volume and transmission time analyzed as shown in the table below. The HSTX transmission speed is Fosc/4, specifically 894.886 kHz at Fosc 3.579545 MHz and 1382.4 kHz at Fosc 5.5296 MHz. As HSTX employs the UART protocol, each 8-bit data requires 11 bits of transmission. Thus, the actual HSTX transmission speed is calculated as Fosc/4/11 × 8, yielding 650826 at Fosc 3.579545 MHz.

number of channels	intermediate buffer configure	bit width of transmission	semi-fulfilling point	Half-full data volume (bits)	Half-full interrupt time (ms)	SPI velocity	SPI half-full data transmission time (ms)	HSTX Speed @Fosc3.579545 MH z	HSTX half-full data transmission time (ms)
1	4x buffer	16	128	2048	40	1200000	1.71	650826	3.15
2	4x buffer	16	128	2048	20	1200000	1.71	650826	3.15
3	4x buffer	16	96	1536	10	1200000	1.28	650826	2.36
1	double buffer	16	128	2048	20	1200000	1.71	650826	3.15
2	double buffer	16	128	2048	10	1200000	1.71	650826	3.15
3	double buffer	16	96	1536	5	1200000	1.28	650826	2.36
1	Cache all	16	128	2048	10	1200000	1.71	650826	3.15

2	Cache all	16	128	2048	5	1200000	1.71	650826	3.15
3	Cache all	16	96	1536	2.5	1200000	1.28	650826	2.36

The waveform data is processed into 16-bit transmission, with its data volume and transmission time analyzed as shown in the table below:

number of channels	**intermediate buffer configure**	**bit width of transmission**	**semi-fulfilling point**	**Half-full data volume (bits)**	**Half-full interrupt time (ms)**	**SPI velocity**	**SPI half-full data transmission time (ms)**	**HSTX Speed @Fosc 3.579545MHz**	**HSTX half-full data transmission time (ms)**
1	4x buffer	24	128	3072	40	1200000	2.56	650826	4.72
2	4x buffer	24	128	3072	20	1200000	2.56	650826	4.72
3	4x buffer	24	96	2304	10	1200000	1.92	650826	3.54
1	double buffer	24	128	3072	20	1200000	2.56	650826	4.72
2	double buffer	24	128	3072	10	1200000	2.56	650826	4.72
3	double buffer	24	96	2304	5	1200000	1.92	650826	3.54
1	Cache all	24	128	3072	10	1200000	2.56	650826	4.72
2	Cache all	24	128	3072	5	1200000	2.56	650826	4.72
3	Cache all	24	96	2304	2.5	1200000	1.92	650826	3.54

The table above shows that when using the three-channel maximum speed buffer, the HSTX interface cannot achieve real-time waveform output for ping-pong operations with a 24-bit waveform length.

When using the waveform data of two channels (current and voltage) with the current channel transmitting 24-bit and the voltage channel transmitting 16-bit (the standard configuration for HSTX interface), the data transmission volume and time analysis are shown in the table below:

number of channels	**Wave frequency (Hz)**	**semi-fulfilling point**	**Half-full data volume (bits)**	**Half-full interrupt time (ms)**	**SPI velocity**	**SPI half-full data transmission time (ms)**	**HSTX Speed @Fosc3.579545MHz**	**HSTX half-full data transmission time (ms)**

2	4x buffer	128	2560	20	12000 00	2.13	650826	3.93
2	double buffer	128	2560	10	12000 00	2.13	650826	3.93
2	Cache all	128	2560	5	12000 00	2.13	650826	3.93

The analysis above demonstrates that, regardless of the caching mechanism or transmission method employed, both SPI and HSTX can deliver real-time waveform outputs for ping-pong operations.

2.13.3 Cache Address Mapping

single channel cache

address mapping	BANK	WAVECON[3:0]，WAVECON[4]=X		
		0x2	0x3	0x1
00H	BANK0	IA	IB	UA
3FH				
40H				
7FH				
80H	BANK1			
BFH				
C0H				
FFH				

dual channel cache

channel gap buffer

address mapping	BANK	WAVECON[3:0]，WAVECON[4]=1		
		0 x 6	0x7	0x8
00H	BANK0	IA	IA	IB
3FH				
40H		UA	IB	UA
7FH				
80H	BANK1	IA	IA	IB
BFH				
C0H		UA	IB	UA
FFH				

channel crossing buffer

address mapping	BANK	WAVECON[3:0]，WAVECON[4]=0		
		0x6	0x7	0x8
00H	BANK0	IA0	IA0	IB0
01H		UA0	IB0	UA0
…		…	…	…
7EH		IA63	IA63	IB63

7FH		UA63	IB63	UA63
80H	BANK1	IA64	IA64	IB64
81H		UA64	IB64	UA64
…		…	…	…
FEH		IA127	IA127	IB127
FFH		UA127	IB127	UA127

The table above shows the channel cross-cache address mapping, where IAn denotes the n-th acquisition data from the IA channel, IBn from the IB channel, and UAn from the UA channel.

three channel buffer

channel gap buffer

address mapping	BANK	WAVECON[3:0]，WAVECON[4]=1
		0xD
00H	BANK0	IA
…		
1FH		
20H		IB
…		
3FH		
40H		UA
…		
5FH		
60H	BANK1	IA
…		
7FH		
80H		IB
…		
9FH		
A0H		UA
…		
BFH		
…		
FFH		

channel crossing buffer

address mapping	BANK	WAVECON[3:0]，WAVECON[4]=0
		0xD
00H	BANK0	IA0
01H		IB0
02H		UA0
…		…
5CH		IA31
5EH		IB31
5FH		UA31

60H	BANK1	IA32
61H		IB32
62H		UA32
…		…
BCH		IA63
BEH		IB63
BFH		UA63
…		
FFH		

2.13.4 Cache and Read Commands

waveform buffer start stop command

The host initiates the waveform buffer operation by transmitting a special command byte (2 bytes) followed by channel selection (1 byte) and read checksum (1 byte). Upon receiving this command, the MKE101R activates or deactivates the buffer according to WAVECOM configuration, as illustrated in the diagram below.

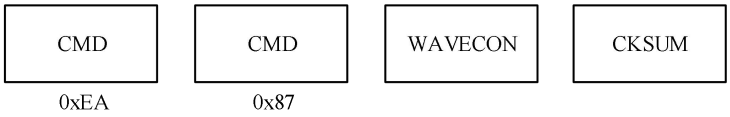


Figure 2-11 Start and Stop Command Frame Format

The command word WAVECON in the waveform buffer command is defined as follows:

- WAVECON[7]: Set to 0 to enable waveform buffering, or 1 to disable it. When 1 is set, the value of WAVECON[6:0] is ignored.
- WAVECON[6]: =0 for single buffer (stop after storage); =1 for continuous buffer.
- WAVECON[5]: Reserved
- WAVECON[4]: Cache mode selection. Valid only with dual-channel cache. =0: Select channel cross cache; =1: Select channel interleaved cache.
- WAVECON[3:0]: Cache channel and cache sequence selection. The corresponding cache channels and sequences are shown in the table below:

WAVECON[3:0]	Cache channels and order (cache order from left to right)		
0 x 0	Do not start cache		
0 x 1	UA	-	-
0 x 2	IA	-	-
0 x 3	IB	-	-
0 x 4	UA	IA	-
0 x 5	UA	IB	-
0 x 6	IA	UA	-
0 x 7	IA	IB	-
0 x 8	IB	UA	-

0 x 9	IB	IA	-
0 x A	UA	IA	IB
0 x B	UA	IB	IA
0 x C	IA	UA	IB
0 x D	IA	IB	UA
0 x E	IB	IA	UA
0 x F	IB	UA	IA

matters need attention ：

1、Before writing the startup command, the clock gate control for the ADC waveform buffer must be enabled via the clock control register CLKCON.

2、When the waveform buffer is active, the host initiates the command, the read is invalid, returns data 0, and the read pointer remains unchanged.

3、To switch between single or continuous waveform buffering, stop the buffering first.

Read waveform buffer pointer address configuration command

The host initiates the configuration of the read waveform pointer address by sending a special command byte (2 bytes) followed by the pointer address (1 byte) and the checksum byte (1 byte). Upon receiving this command, the MKE101R sets the read buffer pointer address to RP_ADDR, as illustrated in the diagram below.

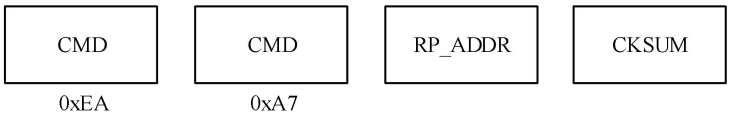


Figure 2-12 Command Frame Format for Pointer Address Configuration

After the read pointer address is configured, if the host initiates a single read of waveform data, the slave will return the corresponding cache address data. Upon completion of the read, the pointer automatically increments by 1, where RP_ADDR is the read pointer address of the SRAM.

single read waveform command

The host initiates a single read operation by first transmitting a special command byte (2 bytes). Upon receiving this command, the MKE101R transmits a read data byte (2 bytes) and a read checksum byte (1 byte), as illustrated in the figure below.

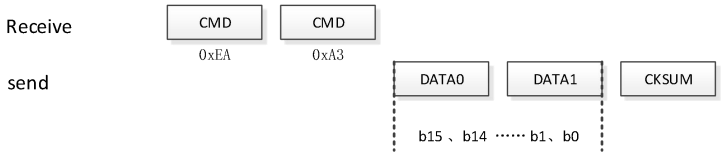


Figure 2-13 Single Read Waveform Command Frame Format

matters need attention ：

1、After each waveform reading, the corresponding read pointer increments by 1. When the last address is read, the read pointer resets to the starting position.

continuous read waveform command

The continuous read operation is initiated by the host, which first transmits a special command byte (2 bytes) followed by the start address (1 byte), end address (1 byte), and checksum (1 byte).

The MKE101R determines whether the command check passes. If passed, it returns a successful command receipt (0x54), then transmits the read data byte (nByte), and finally sends the read checksum byte. If the command check fails, it returns a failed command receipt (0x7F) and stops transmitting subsequent data. As shown in the figure below:

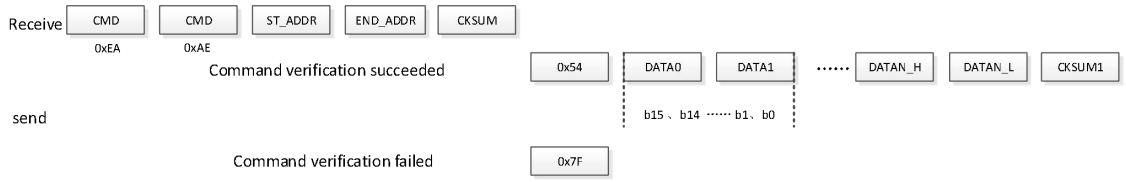


Figure 2-14 Continuous Read Waveform Command Frame Format

matters need attention ：

1、The host sends a checksum CHKSUM (CHKSUM = ~(0xEA+0xAE+ST_ADDR+END_ADDR)) after the command. The slave checks the checksum to confirm command reception. If successful, it sends an ACK (0x54) response, then transmits the read data (length determined by ST_ADDR and END_ADDR), and finally sends the second checksum CHKSUM1.

2、CHKSUM 1 (CHKSUM1 = ~(DATA0+...+DATAn)) excludes ACK from its verification scope, focusing solely on waveform data validation.

3、If the slave detects a checksum error in the masters command, it returns an ACK (0x7F) indicating failure and terminates the command.

4、When the address exceeds the boundary, the transmission is deemed failed, and the failure flag 0x7F is returned.

5、The slave computer calculates and sends the data frame checksum, and the host computer determines whether the data frame transmission is successful based on the checksum.

6、ST_ADDR and END_ADDR must be within the range of 0 to 155, with END_ADDR being greater than or equal to ST_ADDR.

7、After the command is successfully executed, the read pointer stops at END_ADDR+1.

half bit read wave command

The half-read waveform command is only valid in SPI communication mode. After the host activates SCSN, it first writes a special command byte (2 bytes) via SPI, followed by the checksum (1 byte). Upon receiving the read command, the slave device outputs data bit by bit from the SDO pin during the rising edge of SCLK, as shown in the figure below.

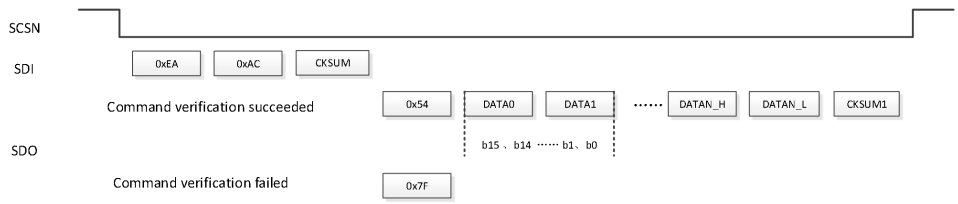


Figure 2-15 Half-read waveform command frame format

matters need attention ：

1. The host sends a command followed by an 8-bit checksum (CHKSUM). The slave checks the CHKSUM to verify command transmission success. If successful, it returns the success flag 0x54, then transmits waveform data and the checksum. If verification fails, it returns the failure flag 0x7F.
2. After successful machine calibration, the system continuously outputs 78 consecutive waveform data points. Each data point read increments the read pointer by 1. Assuming the read pointer address is RP_ADDR before command initiation, the system reads waveforms from RP_ADDR to (RP_ADDR+77) after command execution, with the pointer settling at (RP_ADDR+78) upon command completion. A loop design ensures that if the pointer exceeds the boundary 0x9B, it resets to 0x00 and resumes reading.
3. After transmitting the waveform of the specified length, an 8-bit checksum is immediately sent. The checksum does not include the ACK, but only verifies the waveform data.
4. For every 16-bit waveform data, transmit the high bits first, then the low bits.

2.13.5 Waveform Buffer Application Description

●SPI Communication Waveform Buffer Application:

1、During configuration, the clock control register CLKCON activates the ADC waveform buffer clock gating.

2、Configure waveform buffer half full interrupt and data overwrite error interrupt;

3、Configure WAVECOMs caching mode, such as U/IA dual-channel continuous waveform caching, and enable waveform caching.

4、When the waveform buffer reaches half full, a half-full interrupt is generated, and the MCU triggers an INT interrupt as IRQ_N transitions from high to low.

5、The MCU reads the WAVE_HF_IF register via SPI, clears it, and sets IRQ_N back to high level.

6、The MCU reads continuous waveform data in either continuous or half-block mode using special commands (recommended SPI_SCLK frequency should be no less than 600kHz).

7、The MCU processes data according to the waveform buffer format to obtain complete waveforms for both U and IA channels.

8、The MCU performs power quality analysis through complete continuous waveforms, including FFT, abrupt rises and falls, flicker, and other characteristics.

9、The WAVECOM[7] module in WAVECOM can disable waveform buffering.

●UART communication waveform buffer application:

1、During configuration, the clock control register CLKCON activates the ADC waveform

buffer clock gating.

2、Configure WAVECOMs caching mode: for IA channels, enable single-channel waveform caching (UART interface supports only single-channel caching), and activate waveform caching.

3、When the buffer reaches full capacity (refer to the buffer schedule), the waveform buffering will automatically stop.

4、The MCU configures the pointer address of the read buffer through special commands and reads the waveform data in either single or consecutive modes.

5、The user can analyze the waveform of the output half-wave or full-wave data.

●HSTX communication waveform buffer application:

be continued

2.14 Checksum and CRC (Cyclic Redundancy Check)

2.14.1 Scope of Validation

address	name	R/W	word length	Reset value	checksum range	CRC check range	CRC check sequence
meter register and metering control register					MKE101R	MKE101R	MKE101R
00H	SYSCON	R/W	2	0003h	√	√	1
01H	EMUCON	R/W	2	0003h	√	√	2
02H	HFConst	R/W	2	1000h	√	√	3
03H	PStart	R/W	2	0060h	√	√	4
04H	DStart	R/W	2	0120h	√	√	5
05H	GPQA	R/W	2	0000h	√	√	6
06H	GPQB	R/W	2	0000h	√	√	7
07H	PhsA	R/W	1	00h	√	√	8
08H	PhsB	R/W	1	00h	√	√	9
09H	QPhsCal	R/W	2	0000h	√	√	10
0AH	APOSA	R/W	2	0000h	√	√	11
0BH	APOSB	R/W	2	0000h	√	√	12
0CH	RPOSA	R/W	2	0000h	√	√	13
0DH	RPOSB	R/W	2	0000h	√	√	14
0EH	IARMSOS	R/W	2	0000h	√	√	15
0FH	IBRMSOS	R/W	2	0000h	√	√	16
10H	IBGain	R/W	2	0000h	√	√	17
13H	DCIAH	R/W	2	0000h	√	√	18
14H	DCIBH	R/W	2	0000h	√	√	19
15H	DCUH	R/W	2	0000h	√	√	20

16H	DCL	R/W	2	0000h	√	√	21
17H	EMUCON2	R/W	2	0000h	√	√	22
18H	QPhsCal 2	R/W	2	0000h	√	√	23
19H	SYSCON2	R/W	2	0000h	√	√	24
1AH	CLKCON	R/W	2	0000h	√	√	25
1BH	HFConst2	R/W	2	0000h	√	√	26
1CH	HFConst3	R/W	2	0000h	√	√	27
5EH	GFS	R/W	2	0000h	√	√	28
60H	EMUCON3	R/W	2	0000h	√	√	29
61H	EMUCON4	R/W	2	0000h	√	√	30
62H	EMUCON5	R/W	2	0000h	√	√	31
63H	EMUCON6	R/W	2	0000h	√	√	32
64H	PINCFG	R/W	2	0000h	√	√	33
67H	PPhsCalA	R/W	2	0000h	√	√	34
68H	PPhsCalB	R/W	2	0000h	√	√	35
69H	HWCFG	R/W	2	0000h	√	√	36
6BH	SWAVECFG1	R/W	2	0000h	√	√	37
6CH	SWAVECFG2	R/W	2	0000h	√	√	38
6DH	Swave_PHSIA	R/W	2	0000h	√	√	39
6EH	Swave_PHSIB	R/W	2	0000h	√	√	40
6FH	Swave_PHSU	R/W	2	0000h	√	√	41
70H	Swave_GSIA	R/W	2	0000h	√	√	42
71H	Swave_GSIB	R/W	2	0000h	√	√	43
72H	Swave_GSU	R/W	2	0000h	√	√	44
73H	GFP	R/W	2	0000h	√	√	45
74H	FPOS	R/W	2	0000h	√	√	46
75H	IBTH	R/W	2	0000h	√	√	47
Extend the register group using the extension command							
00H (Extended)	IIC_CFG	RW	2	0014h	×	√	55
20H (Extended)	WAVECFG	RW	1	00h	×	√	56
21H (Extended)	HSTX_CTL	RW	3	000000h	×	√	57.58 (high first)
22H (Extended)	HSTX_RES_OE	RW	2	0000h	×	√	59
23H (Extended)	HSTX_EN	RW	1	00h	×	√	60
24H (Extended)	HSTX_PFDAT	RW	4	800A20AAh	×	√	61,62 (Calculate the higher value first)

25H (Extended)	HSTX_QFDAT	RW	4	800C40CCh	×	√	63,64 (Calculate the higher value first)
26H (Extended)	HSTX_FPFDAT	RW	4	800E60EEh	×	√	65,66 (Start with the higher value)
27H (Extended)	HSTX_IRQDAT	RW	4	800820A8h	×	√	67,68 (Start with the higher value)
28H (Extended)	continue to have	RW	2	0000h	×	√	69
29H (Extended)	continue to have	RW	1	07h	×	√	70
2AH (Extended)	continue to have	RW	1	00h	×	√	71
2BH (expanded)	HSTX_TXOUT	RW	1	00h	×	√	72
2CH (Extended)	HSTX_IOCFG	RW	4	00000610h	×	√	73,74 (high first)
32H (Extended)	ZXOTU	R/W	2	0000h	√	√	48
33H (Extended)	USAG	R/W	2	0000h	√	√	49
3 4H (Extended)	UPEAK	R/W	2	0000h	√	√	50
3 5H (Extended)	IAPEAK	R/W	2	0000h	√	√	51
3 6H (Extended)	IBPEAK	R/W	2	0000h	√	√	52
37H (Extended)	GQA	R/W	2	0000h	√	√	53
38H (Extended)	GQB	R/W	2	0000h	√	√	54

2.14.2 Checksum

EMUStatus[15:0] provides a register for storing the 16-bit checksum of calibration parameter configuration. The external MCU can monitor this register to detect potential calibration data corruption, with the verification scope as described in Section 2.14.1.

The checksum algorithm involves double-byte accumulation followed by inversion. For single-byte registers PHSA/PHSB, the process extends to double-byte accumulation with the extended byte set to 00H.

Different communication methods and speeds have different default checksum values upon power-on, as shown in the table below.

communication mode	speed	Default value of power supply
SPI	1.7Mbps	0xEE79
UART	Fosc/2/(15*47+41) bps	0xC079
	Fosc/2/(15*24+13) bps	0xD879
	Fosc/2/(15*12+6) bps	0xE379
	Fosc/2/(15*6+3) bps	0xE979

The checksum calculation will restart under the following three conditions: system reset, write operation on a register within the checksum range, or read operation on the EMUStatus register. Each checksum calculation takes 11.2 microseconds.

2.14.3 CRC Verification Method

Cyclic redundancy check (CRC) is primarily used to verify the integrity of data during transmission or storage. The CRC calculation unit employs a polynomial generator to derive the CRC code from a 16-bit data stream.

When writing and reading the CRC result of the metering key register through SPI or UART, the value of the register is recalculated by CRC16.

- You can choose to verify the calibration data using checksum or CRC-16.
- Supports CRC-16/XMODEM polynomial (formula: CRC16 = $X)^{16}+ X^{12}+ X^5 + 1$, the initial value check is 16 h0000, the XOR remainder is 16 h0000, no input or output data inversion is performed
- A total of 68 registers are involved in the verification process, requiring 74 rounds of CRC16 calculations.
- Supports 16-bit CRC
- For a single-byte register, expand it to double-byte and calculate. The expanded byte is 00H.

For four-byte registers, split them into high 16-bit and low 16-bit double bytes, performing

calculations in two stages. The high double byte is processed first, with the remaining part extended using 00H. There are 68 registers participating in the CRC16 calculation, requiring 74 rounds. The address range and calculation sequence are: non-expanded registers 0x00~0x10 / 0x13~0x1C / 0x5E / 0x60~0x64 / 0x67~0x69 / 0x6B~0x75, and expanded registers 0x32~0x38/0x00/0x20~0x2C. Among these, expanded registers 0x21/0x24~0x27/0x2C require two separate calculation rounds. For single-byte registers, expand them into double bytes before calculation, with the extended byte being 00H. For four-byte registers, split them into high 16-bit and low 16-bit double bytes, performing calculations in two stages, with the high double byte processed first.

communication mode	speed	Default value of power supply	Enable CRC default value
SPI	1.7Mbps	0xA639	0x6B30
UART	Fosc/2/(15*47+41) bps	0xDB7D	0x1674
	Fosc/2/(15*24+13) bps	0xC6C1	0x0BC8
	Fosc/2/(15*12+6) bps	0x9645	0x5B4C
	Fosc/2/(15*6+3) bps	0x912A	0 x5C23

2.14.4 Switching Between Checksum and CRC16 Verification Methods

Typically, the verification method is determined by the system control register 2. SYSCON2[14].CHKSUM_CRC_SEL determines the verification method for calibration data. When writing to the involved registers or reading the verification results, the values are recalculated. However, during each CHKSUM_CRC_SEL switch, both Chksum and CRC16 perform a simultaneous register data verification.

2.15 Register

2.15.1 Register List

Table 2-1 MKE101R Register List

address	name	R/W	word length	Reset value	functional description
meter register and metering control register					
00H	SYSCON	R/W	2	0003h	system control register, write protection
01H	EMUCON	R/W	2	0003h	write protected measurement register
02H	HFConst	R/W	2	1000h	pulse frequency register, write protected

03H	PStart	R/W	2	0060h	Active startup power setting, write protection
04H	DStart	R/W	2	0120h	Customize power-on setting, write protection
05H	GPQA	R/W	2	0000h	Channel A power gain correction register, write protected
06H	GPQB	R/W	2	0000h	Channel B power gain correction register, write protected
07H	PhsA	R/W	1	00h	Channel A phase correction register, write protected
08H	PhsB	R/W	1	00h	Channel B phase correction register, write protected
09H	QPhsCal	R/W	2	0000h	reactive power phase compensation, write protection
0AH	APOSA	R/W	2	0000h	Channel A has an active power offset correction register with write protection
0BH	APOSB	R/W	2	0000h	Channel B has an active power offset correction register with write protection
0CH	RPOSA	R/W	2	0000h	Channel A has a reactive power offset correction register with write protection
0DH	RPOSB	R/W	2	0000h	Channel B reactive power offset correction register with write protection
0EH	IARMSOS	R/W	2	0000h	Channel A current offset compensation with write protection
0FH	IBRMSOS	R/W	2	0000h	Channel B current offset compensation with write protection
10H	IBGain	R/W	2	0000h	Channel B gain setting, write protection
11H	D2FPL	R/W	2	0000h	Write protection is enabled for the lower 16 bits of the custom power register D2FP.
12H	D2FPH	R/W	2	0000h	To configure the high 16-bit of the power register D2FP, the user must first write to D2FPH, then to D2FPL, and finally D2FP will perform power integration and write protection.
13H	DCIAH	R/W	2	0000h	The high 16-bit of the DC offset calibration register in the Ia channel is write-protected.
14H	DCIBH	R/W	2	0000h	The high 16-bit of the IB channel DC offset calibration register is write-protected.
15H	DCUH	R/W	2	0000h	The high 16-bit of the U-channel DC offset correction register is

					write-protected.
16H	DCL	R/W	2	0000h	The lower 4 bits of three DC offset correction registers: DCL[11:0] = {DCU[3:0], DCIBL[3:0], DCIAL[3:0]} with write protection
17H	EMUCON2	R/W	2	0000h	Measurement Control Register 2, Write Protection
18H	QPhsCal 2	R/W	2	0000h	Reactive power phase compensation with write protection. This feature specifically compensates for reactive power (PowerQB), and channel switching does not affect the compensation value.
19H	SYSCON2	R/W	2	0000h	System control register with write protection, sharing the same write protection as SYSCON
1AH	CLKCON	R/W	2	0000h	module clock configuration register
1BH	HFConst2	R/W	2	0000h	The pulse frequency register 2, with write protection, corresponds to the three sets of energy integration units: D2F3, D2F4, and D2F8.
1CH	HFConst3	R/W	2	0000h	The pulse frequency register 3, with write protection, corresponds to the three sets of energy integration units: D2F5, D2F6, and D2F9.
5EH	GFS	R/W	2	0000h	gain register of fundamental voltage and fundamental current
5FH	EXTEND REG	R/W			extended register operation address
60H	EMUCON3	R/W	2	0000h	Measurement control register 3 with write protection, configured for pulse integration unit functions
61H	EMUCON4	R/W	2	0000h	Measurement control register 4 with write protection, configured for pulse integration unit functions
62H	EMUCON5	R/W	2	0000h	Measurement control register 5 with write protection, configured for pulse integration unit functions
63H	EMUCON6	R/W	2	0000h	Measurement control register 6 with write protection, configured for pulse integration unit and fundamental wave correlation functions. See register description for details.

64H	PINCFG	R/W	2	0000h	Each of the three pins (PF, QF, IRQ) is controlled by four bits.
65H	D2FP2L	R/W	2	0000h	The lower 16 bits of the custom power register D2FP2 are write-protected and not involved in checksum calculation.
66H	D2FP2H	R/W	2	0000h	To configure the high 16-bit of the power register D2FP2, the user must first write to D2FP2H, then D2FP2L, and finally D2FP2 to enable power integration and write protection. This process does not participate in checksum verification.
67H	PPhsCalA	R/W	2	0000h	Channel A features active phase compensation using power phase compensation, with write protection enabled.
68H	PPhsCalB	R/W	2	0000h	Channel B features active phase compensation, with power phase compensation mode and write protection.
69H	HWCFG	R/W	2	0000h	Half-wave power and half-wave RMS control registers, see register description for details
6AH	SPCMD	R/W	2	0000h	special command register
6BH	SWAVECFG1	R/W	2	0000h	Control register 1 for synchronous sampling channel, see register description
6CH	SWAVECFG2	R/W	2	0000h	Control register 2 for synchronous sampling channel, see register description
6DH	Swave_PHSIA	R/W	2	0000h	Phase Correction of Synchronous Sampling Channel IA
6EH	Swave_PHSIB	R/W	2	0000h	Phase Correction of Synchronous Sampling Channel IB
6FH	Swave_PHSU	R/W	2	0000h	Phase Correction of Synchronous Sampling Channel U
70H	Swave_GSIA	R/W	2	0000h	Gain Correction of Synchronous Sampling Channel IA
71H	Swave_GSIB	R/W	2	0000h	Gain Correction of Synchronous Sampling Channel IB
72H	Swave_GSU	R/W	2	0000h	Gain Correction of Synchronous Sampling Channel U
73H	GFP	R/W	2	0000h	fundamental active power gain correction register

74H	FPOS	R/W	2	0000h	fundamental active power offset correction register
75H	IBTH	R/W	2	0000h	The IB channel half-wave RMS threshold register is a 16-bit register.
interrupt register					
40H	IE	R/W	1	00h	interrupt enable register, write protection
41H	IF	R	1	00h	interrupt flag register, clear after reading
42H	RIF	R	1	00h	Reset the interrupt status register and clear it after reading
state register					
43H	SysStatus	R	1	--	state register
44H	RData	R	4	--	Last SPI/UART readout data
45H	WData	R	2	--	Last SPI/UART write data
46H	WAVE_IF	RC	1	00h	waveform buffer status flag register
47H	WAVE_IE	RW	1	00h	waveform buffer interrupt enable register
7EH	DeviceID2	R	3	820904h	Device ID2
7FH	DeviceID	R	3	820900h	Device ID
Extend the register group using the extension command 0x5FH					
00H (Extended)	IIC_CFG	RW	2	0014h	IIC configuration register
01H (Extended)	IIC_CTL	RW	2	0000h	IIC control register
02H (Extended)	IIC_STA	RW	2	0000h	IIC status control register
03H (Extended)	IIC_SADDR	RW	2	0000h	IIC from device address register
04H (Extended)	IIC_TRDAT0	RW	2	0000h	IIC Data Register 0
05H (Extended)	IIC_TRDAT1	RW	2	0000h	IIC Data Transceiver Register 1
06H (Extended)	IIC_TRDAT2	RW	2	0000h	IIC Data Transceiver Register 2
07H (Extended)	IIC_TRDAT3	RW	2	0000h	IIC Data Transceiver Register 3
08H (Extended)	IIC_TRDAT4	RW	2	0000h	IIC Data Transceiver Register 4
09H (Extended)	IIC_TRDAT5	RW	2	0000h	IIC Data Transceiver Register 5
20H (Extended)	WAVE_CTL	RW	1	00h	waveform output control register
21H (Extended)	HSTX_CTL	RW	3	000000h	HSTX control register

22H (Extended)	HSTX_REG_OE	RW	2	0000h	HSTX meter register output enable register
23H (Extended)	HSTX_EN	RW	1	00h	HSTX enable register
24H (Extended)	HSTX_PFDAT	RW	4	800A20AAh	HSTX PF Reference Value Register
25H (Extended)	HSTX_QFDAT	RW	4	800C40CCh	HSTX QF Reference Value Register
26H (Extended)	HSTX_FPFDAT	RW	4	800E60EEh	HSTX FPF reference value register
27H (Extended)	HSTX_IRQDAT	RW	4	800820A8h	HSTX interrupt data reference register
28H (Extended)	continue to have	RW	2	0000h	continue to have
29H (Extended)	continue to have	RW	1	07h	continue to have
2AH (Extended)	continue to have	RW	1	00h	continue to have
2BH (expanded)	HSTX_TXOUT	RW	1	00h	HSTX Pin Function Enable Register
2CH (Extended)	HSTX_IOCFG	RW	4	00000610h	HSTX output pulse select register
30H (Extended)	IBDET_CFG	RW	1	03h	leakage current protection configuration register
31H (Extended)	IBDET_FLG	RW	1	00h	leakage current detection flag register
32H (Extended)	ZXOTU	R/W	2	0000h	Set the zero-crossing threshold register. The zero-crossing signal is generated only when the high 16 bits of the valid value exceed this threshold, ensuring the voltage line frequency is correct. The default value is 0, which corresponds to 16h100.
33H (Extended)	USAG	R/W	2	0000h	voltage drop threshold register
3 4H (Extended)	UPEAK	R/W	2	0000h	U-channel voltage overvoltage threshold register
3 5H (Extended)	IAPEAK	R/W	2	0000h	IA channel current overload threshold register
3 6H (Extended)	IBPEAK	R/W	2	0000h	IB channel current overload threshold register
37H	GQA	R/W	2	0000h	Channel A reactive power gain register

(Extended)					
38H (Extended)	GQB	R/W	2	0000h	Channel B reactive power gain register
parameter register					
address	name	R/W	word length	Reset value	functional description
20H	PFCnt	R/W	2	0000h	Fast active pulse counting, write protection
21H	DFcnt	R/W	2	0000h	Customizable fast pulse counting for electrical energy with write protection
22H	IARMS	R	3	000000h	effective value of channel A current
23H	IBRMS	R	3	000000h	effective value of channel B current
24H	URMS	R	3	000000h	voltage effective value
25H	UFreq	R	2	0000h	frequency of voltage
26H	PowerPA	R	4	00000000h	active power PA
27H	PowerPB	R	4	00000000h	active power PB
28H	PowerQ	R	4	00000000h	reactive power QA
29H	EnergyP	R	3	000000h	The function has a reset option: it can be reset or not reset after reading. The default setting is non-reset, controlled by the EnergyCLR register bit.
2AH	EnergyP2	R	3	000000h	The function includes reading and clearing the register, with the power freeze register being optional. By default, the register is cleared after reading.
2BH	EnergyD	R	3	000000h	No functional energy or custom energy. The system defaults to non-resetting after reading, with the EnergyCLR register bit controlling the reset option.
2CH	EnergyD2	R	3	000000h	No functional quantity or custom energy. The read-clear register and power freeze register are optional, with the read-clear register being the default setting.
2DH	EMUStatus	R	3	00EE79h	Measurement State and Check Register
2EH	EMUStatus2	R	3	000000h	Measurement status register 2{CRC[15:0],3h0, IBTH_FLAG, hwfrms_up, hwrms_up, bgrok, vref_ok} See details below

2FH	EMUStatus3	R	4	0000000H	Measurement status register 3, see {swave_time[9:0], CF9, CF8, CF7, CF6, CF5, CF4, CF3, Nopld9, Nopld8, Nopld7, Nopld6, Nopld5, Nopld4, Nopld3, REVP9, REVP8, REVP7, REVP6, REVP5, REVP4, REVP3, 1b1}
30H	SPL_IA	R	3	000000h	The ADC samples in the I/A channel are 20-bit signed numbers using twos complement format, with the high two bits as sign bits. The data refresh rate is Fosc/2/128,2 1.6 kHz z@5.5296 MHz z
31H	SPL_IB	R	3	000000h	The IB channel ADC samples 20-bit signed numbers in twos complement format, with the high two bits as sign bits. The data refresh rate is F osc/2/128,2 1.6 kHz at 5.5296 MHz.
32H	SPL_U	R	3	000000h	The U-channel ADC samples values with 20-bit signed numbers using twos complement format, where the high two bits serve as the sign bit. The data refresh rate is F osc/2/128, with a clock frequency of 2 1.6 kHz and a clock period of 5.5296 μs.
34H	ZXFCNT	R	2	0000h	When the software executes the zero-crossing measurement command (0xEA/0x7C), the metering chip uses the commands execution time as a reference point. It then calculates the time difference between the voltages zero-crossing and this reference point, with the result stored in the designated register.
35H	UFreq2	R	3	000000h	The voltage frequency register 2 extends the frequency measurement range, with the value at 50Hz matching that of UFreq (0x25H).
36H	PowerQB	R	4	00000000h	reactive power QB
37H	Energy3	R	3	000000h	The energy register of the third set of integral units D2F3 can be read and reset. The default setting is read-only, with reset option available, controlled by the EnergyCLR register bit.

38H	Energy4	R	3	000000h	The energy register of the fourth integration unit D2F4 can be read and reset. The default setting is read-only, controlled by the EnergyCLR register bit.
39H	Energy5	R	3	000000h	The energy register in the fifth integration unit D2F5 can be read and reset. The default setting is read-only, controlled by the EnergyCLR register bit.
3AH	Energy6	R	3	000000h	The energy register in the sixth integration unit D2F6 can be read and reset. The default setting is read-only, controlled by the EnergyCLR register bit.
3BH	Energy7	R	3	000000h	The energy register in the seventh set of integral units D2F7 can be read and reset. The default setting is read-only, with reset option available, controlled by the EnergyCLR register bit.
3CH	Energy8	R	3	000000h	The energy register in the eighth integration unit D2F8 features an optional read-clear function. The default setting is read-clear, controlled by the EnergyCLR register bit.
3DH	Energy9	R	3	000000h	The energy register in the ninth integral unit D2F9 can be read and reset. The default setting is read-only, controlled by the EnergyCLR register bit.
3EH	PFcnt3	R/W	2	0000h	Fast pulse counting with write protection for the third set of integration units D2F3
3FH	PFcnt4	R/W	2	0000h	Fast pulse counting with write protection for the fourth integration unit D2F4
48H	PFcnt5	R/W	2	0000h	Fast pulse counting with write protection for the fifth integration unit D2F5
49H	PFcnt6	R/W	2	0000h	Fast pulse counting with write protection for the sixth set of integration units D2F6
4AH	PFcnt7	R/W	2	0000h	Quick pulse counting with write protection for the seventh set of integral units D2F7

4BH	PFcnt8	R/W	2	0000h	Fast pulse counting with write protection for the eighth integration unit D2F8
4CH	PFcnt9	R/W	2	0000h	Fast pulse counting with write protection for the ninth integration unit D2F9
4DH	HW_PA	R	4	00000000h	The full-wave active power A with half-cycle updates, including the optional output synchronization sampling channel and metering channel calculated half-wave power
4EH	HW_QA	R	4	00000000h	The full-wave reactive power A, which is updated semi-periodically, originates from the half-wave power calculated by the metering channel.
4FH	HW_IA	R	3	000000 h	The Effective Value of Full-wave IA Channel with Semi-periodic Update
76H	HW_IBTH	R	3	000000 h	When the half-wave RMS value of the IB channel exceeds the threshold IBTH, it is cached in this register.
77H	HW_IB	R	3	000000 h	The Full-wave IB Channel Efficiency with Semi-periodic Update
78H	HW_U	R	3	000000 h	The Effective Value of Full-wave U-channel with Semi-periodic Update
79H	HW_FU	R	3	000000 h	The Effective Value of the Fundamental Wave U Channel with Semi-periodic Update
7AH	HW_FI	R	3	000000 h	The RMS value of the fundamental I channel with half-cycle update
7BH	HW_FP	R	4	00000000 h	active power of fundamental wave with half-period update
7CH	SPL_FU	R	4	00000000 h	Controlled by splf_mode[1:0], it outputs either the instantaneous sampling waveform of the fundamental frequency or the voltage sampling data at two points before and after zero-crossing. For details, refer to the register description.
7DH	SPL_FI	R	4	00000000 h	

2.15.2 Calibration Parameter Registers

System control registers SYSCON/SYSCON2 (0x00/0x19)

<table>
<tr><th colspan="3">SYSTEM Control Register (SYSCON) Address: 0x00 H Default Value: 0003H</th></tr>
<tr><th>bit</th><th>Position Name</th><th>functional description</th></tr>
<tr><td>15</td><td>continue to have</td><td>The default is 0. Do not write 1 to this position.</td></tr>
<tr><td>[14:8]</td><td>Uartbr[6:0]</td><td>The UART baud rate is set to read-only mode, with its value determined by hardware pins B1 and B0.
{B1, B0}=00, Uadrbr=7h2E, Fosc/2/(15*47+41) baud rate
{B1, B0}=01, Uadrbr=7h16, Fosc/2/(15*24+13) baud rate
{B1, B0}=10, Uadrbr=7h0B, Fosc/2/(15*12+6) baud rate
{B1, B0}=11, Uadrbr=7h05, Fosc/2/(15*6+3) baud rate
This only applies when the communication port is set to UART; it reads zero when SPI is selected.
Note: When UART[6:0] is selected as the communication port, it will affect the checksum and CRC calculation results.</td></tr>
<tr><td>7</td><td>continue to have</td><td>The default is 0. Do not write 1 to this position.</td></tr>
<tr><td>6</td><td>ADC2ON</td><td>ADC2ON =1: Enables ADC current channel B; =0: Disables ADC current channel B, keeping the ADC output at 0.</td></tr>
<tr><td>[5:4]</td><td>PGAIB[1:0]</td><td>Channel B analog gain selection:
<table>
<tr><th>PGAIB1</th><th>PGAIB0</th><th>Channel B</th></tr>
<tr><td>0</td><td>0</td><td>PGA=1</td></tr>
<tr><td>0</td><td>1</td><td>PGA=2</td></tr>
<tr><td>1</td><td>0</td><td>PGA=4</td></tr>
<tr><td>1</td><td>1</td><td>PGA=4</td></tr>
</table></td></tr>
<tr><td>[3:2]</td><td>PGAU[1:0]</td><td>Voltage channel analog gain selection:
<table>
<tr><th>PGAU1</th><th>PGAU0</th><th>voltage channel</th></tr>
<tr><td>0</td><td>0</td><td>PGA=1</td></tr>
<tr><td>0</td><td>1</td><td>PGA=2</td></tr>
<tr><td>1</td><td>0</td><td>PGA=4</td></tr>
<tr><td>1</td><td>1</td><td>PGA=4</td></tr>
</table></td></tr>
<tr><td>[1:0]</td><td>PGAIA[1:0]</td><td>Channel As analog gain selection defaults to 16x, with PGAIA[3:2] linked to SYSCON2[1:0] register.
<table>
<tr><th>PGAIA3</th><th>PGAIA2</th><th>PGAIA1</th><th>PGAIA0</th><th>IA channel gain</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>PGA = 4</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>PGA = 8</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>PGA = 12</td></tr>
</table></td></tr>
</table>

		0	0	1	1	PGA = 16 (default)
		0	1	0	1	PGA = 24
		1	0	1	1	PGA = 32
		Other values				**continue to have**

SYSTEM Control Register (SYSCON2) Address: 0x19 H Default Value: 0000H		
bit	**Position Name**	**functional description**
15	**continue to have**	**Default is 0**
14	CHKSUM_CRC_SEL	configuration register check mode selection bit 0: Use CHKSUM for verification; 1: CRC-16/XMODEM verification method; Note: When switching verification methods, both methods will start verification calculations.
13	ISUM_MOD	=0: The formula for calculating the vector sum and magnitude of vectors iA and iB is iA + iB =1: The formula for calculating the vector sum and magnitude of vectors iA and iB is iA-iB
12	ISUM_EN	=0: The IBRMS (23H) register outputs the valid value of the IB channel; =1: The IBRMS (23H) register outputs the vector sum and RMS value of ia and ib;
[11:4]	USAG_CFG	usag_cfg[7:0] sets the half-cycle count for voltage drop detection
3	SAG_EN	SAG_EN=1: Enables SAG/SWELL-related functions and activates the leakage-related register. SAG_EN=0: The SAG/SWELL functions are disabled, and the associated registers remain reserved.
2	Sag_Freq_sel	=0: SAG (Voltage Sag) cycle for 50Hz applications, =1: SAG (Voltage Sag) cycle for 60Hz applications
1	PGAIA3	Together with the lowest two bits of the SYSCON register, PGAIA[1:0], they form a 4-bit register that determines the PGA of the IA channel.
0	PGAIA2	

Measurement Control Registers EMUCON/EMUCON2 (0x01/0x17)

The metering control register is used to set the metering function.

Energy Measure Control Register (EMUCON) Address: 0x01 H Default Value: 0003H		
bit	**Position Name**	**functional description**
15	EnergyCLR	Default is 0 EnergyCLR =0: The 29/2B energy register is of the accumulator type. EnergyCLR =1: The 29/2B power register is a read-only type with zero-clearing capability.

<table>
<tr><td>14</td><td>HPFIBOFF</td><td>HPFIBOFF=0: Enables the digital high-pass filter for the IB channel
HPFIBOFF=1: Disables the digital high-pass filter for the IB channel</td></tr>
<tr><td>[13:12]</td><td>QMOD[1:0]</td><td>Custom energy accumulation method selection:
<table>
<tr><td>QMOD1</td><td>QMOD0</td><td>cumulative power Qm</td></tr>
<tr><td>0</td><td>0</td><td>Qm=DataQ, representing algebraic summation mode where both forward and reverse power are accumulated. Forward power increments Dfcnt, while reverse power decrements it. Negative power is indicated by the REVQ symbol.</td></tr>
<tr><td>0</td><td>1</td><td>Only positive power is accumulated. The positive power method involves adding Dfcnt, while the reverse power does not participate in the integration.</td></tr>
<tr><td>1</td><td>0</td><td>Qm=|DataQ| adopts absolute value calculation, with both forward and reverse power values being accumulated. Both forward and reverse Dfcnt are summed without negative power sign indication.</td></tr>
<tr><td>1</td><td>1</td><td>The reverse power mode only accumulates reverse power, during which Pfcnt decreases, while forward power is not integrated.</td></tr>
</table></td></tr>
<tr><td>[11:10]</td><td>PMOD[1:0]</td><td>Functionally cumulative method selection: Custom energy accumulation method as in the table above.</td></tr>
<tr><td>9</td><td>ZXD1</td><td>The initial value of ZX output is 0. Depending on the configuration of ZXD1 and ZXD0, it outputs different waveforms:
ZXD1=0 indicates that the ZX output changes only at the selected zero-crossing points.
ZXD1=1 indicates that the ZX output changes at both positive and negative zero-crossing points.</td></tr>
<tr><td>8</td><td>ZXD0</td><td>ZXD0=0, indicating the forward zero-crossing point is selected as the zero-crossing detection signal.
ZXD0=1 indicates the selection of a negative zero-crossing point as the zero-crossing detection signal.</td></tr>
<tr><td>7</td><td>ZXCFG</td><td>ZXCFG =0: The ZX pin IRQ_N is used as IRQ_N.
ZXCFG =1: The ZX pin IRQ_N /ZX is designated as ZX.</td></tr>
<tr><td>6</td><td>HPFIAOFF</td><td>HPFIAOFF=0: Enable digital high-pass filter for IA channel
HPFIAOFF=1: Turn off the digital high-pass filter for the IA channel</td></tr>
<tr><td>5</td><td>HPFUOFF</td><td>HPFUOFF=0: Enables the U-channel digital high-pass filter
HPFUOFF=1: Turn off the U-channel digital high-pass filter</td></tr>
<tr><td>4</td><td>CFSUEN</td><td>CFSUEN is the control bit for the PF/QF pulse output acceleration module. When CFSUEN=1, the pulse acceleration module is enabled, increasing the pulse output rate by 2^(CFSU[1:0]+1) times. When</td></tr>
</table>

		CFSUEN=0, the pulse acceleration module is disabled, and the pulse is output normally.
[3:2]	CFSU[1:0]	This product is intended for use in conjunction with CFSUEN. Refer to the CFSUEN package insert.
1	DRUN	DRUN=1 enables QF pulse output and custom energy register accumulation. DRUN=0, disable QF pulse output and custom energy register accumulation. The default value is 1. Metering is only activated when DRUN is set to 1 and either a write operation is initiated on EMUCON4 (0x61H) or a read operation is performed on any register. Simply setting DRUN to 1 does not trigger metering.
0	PRUN	PRUN=1 enables the PF pulse output and active power register accumulation. PRUN=0, disables PF pulse output and active power register accumulation. The default value is 1. Metering is only activated when PRUN is set to 1 and either a write operation is initiated on EMUCON4 (0x61H) or a read operation is performed on any register. If PRUN is simply set to 1, metering will not commence. This configuration enables multiple integrators to perform integration simultaneously, ensuring consistent performance across all units. It also maintains backward compatibility with MKE101R series software, as the MCU will automatically initiate read operations upon configuration completion.

Energy Measure Control Register2 (EMUCON2) Address: 0x17 H Default Value: 0000H		
bit	**Position Name**	**functional description**
15	QFCFG	QF Pin Output Multiplexing Configuration =0: The default output is QF function; =1: Output as REVP function;
14	continue to have	continue to have
[13:12]	FreqCnt	=00: The frequency measurement is taken over 32 cycles; =01: The frequency measurement is taken over 4 cycles; =10: The frequency measurement is taken over 8 cycles; =11: The frequency measurement is taken over 16 cycles;
11	FreqMode1	=0: Select the voltage channel as the source for ZXCNT zero-crossing event detection. =1: Select current channel A as the source for ZXCNT zero-crossing event detection;
10	FreqMode0	=0: Use the low-pass filtered voltage channel data as the frequency

		measurement source; =1: Use the original voltage channel waveform data as the frequency measurement source.
9	PhsB0	It can be used as the least significant bit and PhsB register (0x08H) to form a 9-bit phase correction register, which improves the phase correction resolution from 0.02°@ F osc 3.579745MHz and 0.013°@ F osc5.5296MHz to 0.01°@ F osc 3.579745MHz and 0.0065°@F osc 5.5296MHz. When this register is 0, it has no effect on phase correction.
8	PhsA0	It can be used as the least significant bit and PhsA register (0x07H) to form a 9-bit phase correction register, which improves the phase correction resolution from 0.02°@ F osc 3.579745MHz and 0.013°@ F osc5.5296MHz to 0.01°@ F osc 3.579745MHz and 0.0065°@F osc 5.5296MHz. When this register is 0, it has no effect on phase correction.
7	UPMODE	=0, the power and RMS value registers are updated at a rate of Fosc/2/2^19; =1, the power and RMS value register update speed is Fosc/2/2^17;
6	ZXMODE	=0, the zero-crossing signal output source is a normally metered voltage signal with no harmonic filtering; =1, the zero-crossing signal output is a low-pass filtered voltage signal.
[5:4]	D2FM[1:0]	=00: Custom power input is set to reactive power; =01: Custom power input is set to the vector sum of active power from channel A and channel B; =10: Set the custom power input to the custom power register D2FP; =11: Custom power input is set to channel B active power;
3	Energy_fz	=0, the power register 2 does not enable the timed freeze function and is reset to zero after reading by default. =1, the power register 2 (addresses 2A and 2C) activates the timed freeze function, loading the value of power register 1 (addresses 29 and 2B) into power register 2 at 2048*1024/Fosc every 581.8711 ms@Fosc3.579545MHz, while simultaneously clearing power register 1.
[2:0]	UPMODE	UPMODE1[2:0]=3h0: The power and RMS value register update speed is determined by EMUCON2.bit7. UPMODE1[2:0]=3h1: The power and RMS value register update speed is Fosc/2/2^15; UPMODE1[2:0]=3h2: The power and RMS value register update speed is Fosc/2/2^16; UPMODE1[2:0]=3h3: The power and RMS value register updates at a rate of Fosc/2/2^17, equivalent to EMUCON2.bit7=1. UPMODE1[2:0]=3h4: The power and RMS value register update speed is Fosc/2/2^18;

		UPMODE1[2:0]=3h5: The power and RMS value register update speed is Fosc/2/2^19, equivalent to EMUCON2.bit7=0; UPMODE1[2:0]=3h6: The power and RMS value register update speed is Fosc/2/2^20; UPMODE1[2:0]=3h7: The power and RMS value register update speed is Fosc/2/2^21;

Pulse frequency registers HFconst/HFconst2/HFconst3 (0x02/0x1B/0x1C)

High Frequency Impulse Const Register (HFConst)				**Address: 0x 02H Default Value : 1000H**				
	Bit15	**14**	**13**	**12**	**11**	**10**	**9**	**Bit8**
Read:	HFC15	HFC14	HFC13	HFC12	HFC11	HFC10	HFC9	HFC8
Write:								
Reset:	0	0	0	1	0	0	0	0
:	**Bit7**	**6**	**5**	**4**	**3**	**2**	**1**	**Bit0**
Read	HFC7	HFC6	HFC5	HFC4	HFC3	HFC2	HFC1	HFC0
Write:								
Reset:	0	0	0	0	0	0	0	0
High Frequency Impulse Const Register (HFConst2)				**Address: 0x 1BH Default Value : 1000H**				
	Bit15	**14**	**13**	**12**	**11**	**10**	**9**	**Bit8**
Read:	HFC15	HFC14	HFC13	HFC12	HFC11	HFC10	HFC9	HFC8
Write:								
Reset:	0	0	0	1	0	0	0	0
:	**Bit7**	**6**	**5**	**4**	**3**	**2**	**1**	**Bit0**
Read	HFC7	HFC6	HFC5	HFC4	HFC3	HFC2	HFC1	HFC0
Write:								
Reset:	0	0	0	0	0	0	0	0
High Frequency Impulse Const Register (HFConst3)				**Address: 0x 1CH Default Value : 1000H**				
	Bit15	**14**	**13**	**12**	**11**	**10**	**9**	**Bit8**
Read:	HFC15	HFC14	HFC13	HFC12	HFC11	HFC10	HFC9	HFC8
Write:								
Reset:	0	0	0	1	0	0	0	0
:	**Bit7**	**6**	**5**	**4**	**3**	**2**	**1**	**Bit0**
Read	HFC7	HFC6	HFC5	HFC4	HFC3	HFC2	HFC1	HFC0
Write:								
Reset:	0	0	0	0	0	0	0	0

HFConst is a 16-bit unsigned number. During comparison, it is evaluated against twice the absolute value of the PFCNT/DFCNT/PFCNT7 register values. If the comparison result equals or exceeds HFConst, the corresponding PF/QF pulse output is triggered. Specifically, HFConst corresponds to three energy integration units: D2F1 (PF), D2F2 (QF), and D2F7.

HFConst2 and HFConst3 function similarly to HFConst, performing verification and calculation

tasks. These registers default to 0x0000H. Specifically, HFConst2 corresponds to the D2F3, D2F4, and D2F8 power integration units, while HFConst3 corresponds to the D2F5, D2F6, and D2F9 units.

Three energy integration units form a complete circuit, each capable of independently measuring forward energy, reverse energy, or combined energy, enabling true bidirectional real-time precision measurement.

Recommended configurations: D2F1/D2F3/D2F5 for full-wave active power; D2F2/D2F4/D2F6 for reactive power; D2F7/D2F8/D2F9 for fundamental active power.

PStart/DStart register (0x03/0x04) for latent start and start-up thresholds

Start Power Threshold Setup Register (PStart)				Address: 0x 03h Default Value : 0060H				
	Bit15	**14**	**13**	**12**	**11**	**10**	**9**	**Bit8**
Read:	PS15	PS 14	PS 13	PS 12	PS11	PS10	PS 9	PS 8
Write:								
Reset:	0	0	0	0	0	0	0	0
	Bit7	**6**	**5**	**4**	**3**	**2**	**1**	**Bit0**
Read:	PS7	PS 6	PS 5	PS 4	PS 3	PS 2	PS 1	PS 0
Write:								
Reset:	0	1	1	0	0	0	0	0

Start Power Threshold Setup Register (DStart)				Address: 0x 04h Default Value : 0120H				
	Bit15	**14**	**13**	**12**	**11**	**10**	**9**	**Bit8**
Read:	QS15	QS 14	QS 13	QS 12	QS11	QS10	QS 9	QS 8
Write:								
Reset:	0	0	0	0	0	0	0	1
	Bit7	**6**	**5**	**4**	**3**	**2**	**1**	**Bit0**
Read:	QS7	QS 6	QS 5	QS 4	QS 3	QS 2	QS 1	QS 0
Write:								
Reset:	0	0	1	0	0	0	0	0

The start threshold is configured by the PStart and DStart registers. These 16-bit unsigned numbers are compared with the absolute values of the high 24 bits of PowerP and DataD (32-bit signed numbers) to determine the start condition.

When PowerP is less than PStart, PF does not output pulses.

When DataD is less than DStart, QF does not output pulses.

PStart corresponds to the integration units D2F1 (default PF), D2F3, D2F5, and D2F7, D2F8, D2F9. When the absolute power value of these units falls below PStart, they will not generate power pulses.

DStart corresponds to the integration units D2F2 (default QF), D2F4, or D2F6. When the absolute power value of these units falls below DStart, they will not generate electrical energy pulses.

Gain correction registers GPQA/GPQB (0x05/0x06)

Power Gain Register A(GPQA)			Address: 0x05h Default Value : 0000H				
	Bit15	14	13	12 … 3	2	1	Bit0
Read: / Write:	GPQA_15	GPQA_14	GPQA_13	GPQA_12…GPQA_3	GPQA_2	GPQA_1	GPQA_0
Reset:	0	0	0	0	0	0	0

Power Gain Register B(GPQB)			Address: 0x06h Default Value : 0000H				
	Bit15	14	13	12 … 3	2	1	Bit0
Read: / Write:	GPQB_15	GPQB_14	GPQB_13	GPQB_12…GPQB_3	GPQB_2	GPQB_1	GPQB_0
Reset:	0	0	0	0	0	0	0

It includes two registers: GPQA and GPQB, which are in twos complement format with the most significant bit as the sign bit.

GPQA corrects the active power in current channel A and voltage channel A, while GPQB corrects the gain in current channel B and voltage channel B.

The correction formula is: P1=P0 (1 + GPQS)

Q1=Q0(1+GPQS)

The GPQS is the normalized value of the gain correction register. For usage, refer to Chapter 3 on calibration methods.

Phase correction registers PhsA/PhsB (0x07~0x08)

Phase Calibration Register A(PhsA)			Address: 0x 07H Default Value : 00H					
	Bit7	6	5	4	3	2	1	Bit0
Read: / Write:	PhsA_7	PhsA_6	PhsA _5	PhsA _4	PhsA _3	PhsA _2	PhsA _1	PhsA _0
Reset:	0	0	0	0	0	0	0	0

Phase Calibration Register B(PhsB)			Address: 0x08 H Default Value : 00H					
	Bit7	6	5	4	3	2	1	Bit0
Read: / Write:	PhsB _7	PhsB _6	PhsB _5	PhsB _4	PhsB _3	PhsB _2	PhsB _1	PhsB _0
Reset:	0	0	0	0	0	0	0	0

Phase correction registers PhsA (for IA and U channels) and PhsB (for IB and U channels). Both registers use signed binary complement, with Bit[7:0] being valid and Bit7 as the sign bit. Refer to Chapter 3 for calibration methods.

One LSB corresponds to a delay of 1/895kHz (1.12 μs/LSB). At 50 Hz, one LSB equals 1.12 μs multiplied by 360.º*50/ 10^6＝0.02º` /LSB phase correction.

Phase correction resolution: 50Hz, 0.02° @F osc 3.579545MHz, 0.013° @ F osc 5.5296MHz

Phase correction range: ±2.56 at 50Hzº@ F osc 3.579545MHz、±1 .65° @ F osc 5.5296MHz

Note: The EMUCON2[9:8] bit in the EMUCON2 register (0x17H) can increase the phase

correction scale to 0.01.º@ F osc 3.579545MHz、0 .0065° @ F osc 5.5296MHz

Reactive power phase compensation registers QPhsCal/QPhsCal2 (0x09/0x18)

Reactive Power Phase Calibration Register (QPhsCal)				Address: 09H		Default Value : 0000H		
	Bit15	14	13	12..3		2	1	Bit0
Read: / Write:	QPC15	QPC14	QPC13	QPC12 QPC3		QPC2	QPC1	QPC0
Reset:	0	0	0	0	0	0	0	0

Reactive Power Phase Calibration Register (QPhsCal2)				Address: 18H		Default Value : 0000H		
	Bit15	14	13	12..3		2	1	Bit0
Read: / Write:	QPC15	QPC14	QPC13	QPC12 QPC3		QPC2	QPC1	QPC0
Reset:	0	0	0	0	0	0	0	0

The reactive power phase compensation register is designed for phase compensation in the 90° phase-shift filter of U-channel during reactive power calculation, and can also correct phase errors in reactive power. It employs a 16-bit binary complement format, with the most significant bit as the sign bit. For usage instructions, refer to Chapter 3: Meter Calibration Methods.

Correction formula: Q2 = Q1-QPs*P1

P1 is the active power, Q1 is the reactive power before compensation, and Q2 is the reactive power after compensation.

Note: When the external crystal oscillator is set to 5.5296MHz and both active phase 1.0 and 0.5L have been calibrated, it is recommended to set Q PhsCalx to the recommended value 0x12C for reactive phase compensation.

Offset correction registers APOSA/APOSB (0x0A/0x0B)

Active Power Offset Register A(APOSA)			Address: 0AH	Default Value : 0000H			
	Bit15	14	13	12 … 3	2	1	Bit0
Read: / Write:	APOSA_15	APOSA _14	APOSA _13	APOSA _12…APOSA _3	APOSA _2	APOSA _1	APOSA _0
Reset:	0	0	0	0	0	0	0

Active Power Offset Register B(APOSB)			Address: 0BH	Default Value : 0000H			
	Bit15	14	13	12 … 3	2	1	Bit0
Read: / Write:	APOSB_15	APOSB _14	APOSB _13	APOSB _12…APOSB _3	APOSB _2	APOSB _1	APOSB _0
Reset:	0	0	0	0	0	0	0

The active offset correction is suitable for precision correction of small signals. Both registers are in twos complement format, with the most significant bit being the sign bit. Refer to Chapter 3 for calibration methods.

The APOSA register stores the active power offset values for current channel A and U channel, while the APOSB register stores the offset values for current channel B and U channel.

Reactive power offset correction registers RPOSA/RPOSB (0x0C/0x0D)

Rective Power Offset Register (RPOSA)			Address: 0CH	Default Value : 0000H			
	Bit15	14	13	12 … 3	2	1	Bit0
Read:	RPOSA_15	RPOSA _14	RPOSA _13	RPOSA _12…RPOSA _3	RPOSA _2	RPOSA _1	RPOSA _0
Write:							
Reset:	0	0	0	0	0	0	0

Rective Power Offset Register (RPOSB)			Address: 0DH	Default Value : 0000H			
	Bit15	14	13	12 … 3	2	1	Bit0
Read:	RPOSB_15	RPOSB _14	RPOSB _13	RPOSB _12…RPOSB _3	RPOSB _2	RPOSB _1	RPOSB _0
Write:							
Reset:	0	0	0	0	0	0	0

The reactive power offset correction register is used to correct the precision of small reactive power signals. Both registers are in twos complement format, with the most significant bit being the sign bit. For usage, refer to Chapter 3: Meter Calibration Methods.

The RPOSA register stores the reactive power offset values for current channel A and U channel, while the RPOSB register stores the reactive power offset values for current channel B and U channel.

Valid Offset Correction Register IARMSOS/IBRMSOS (0x0E/0x0F)

IA RMS Offset Register(IARMSOS)			Address: 0EH	Default Value : 0000H			
	Bit15	14	13	12 … 3	2	1	Bit0
Read:	IARMS_15	IARMS _14	IARMS _13	IARMS _12… IARMS _3	IARMS _2	IARMS _1	IARMS _0
Write:							
Reset:	0	0	0	0	0	0	0

IB RMS Offset Register(IBRMSOS)			Address: 0FH	Default Value : 0000H			
	Bit15	14	13	12 … 3	2	1	Bit0
Read:	IBRMS_15	IBRMS _14	IBRMS _13	IBRMS _12… IBRMS _3	IBRMS _2	IBRMS _1	IBRMS _0
Write:							
Reset:	0	0	0	0	0	0	0

The valid value Offset correction register is used to correct small-signal accuracy for current valid values. Both registers are in twos complement format, with the most significant bit being the sign bit. Refer to Chapter 3 for meter calibration methods.

The IARMSOS register stores the offset value of the effective value of current A, while the IBRMSOS register stores the offset value of the effective value of current B.

When the frmsi_os_en (bit7) of EMUCON4 (0x61H) is set to 0, the IBRMSOS register functions as an Offset correction register for the IB channels valid value, enabling calibration of the IBRMS (0x23) register. When set to 1, it acts as an Offset correction register for the fundamental currents valid value in the HW_FI (0x7A) register.

Channel B gain setting IBGain (0x10)

Current B Gain Register (IBGain)			Address: 10H Default Value : 0000H				
	Bit15	14	13	12 … 3	2	1	Bit0
Read: / Write:	IBG15	IBG14	IBG13	IBG12…IBG3	IBG2	IBG1	IBG0
Reset:	0	0	0	0	0	0	0

The current channel B gain setting register is designed to ensure consistency calibration between the two current channels for anti-theft metering. The calibration is performed at 100% Ib point. For usage instructions, refer to Chapter 3: Meter Calibration Methods.

The channel B current gain register uses binary complement code, the highest bit is the sign bit, which indicates the range (-1, +1).

If IBGain>=2^15, then GainI2= (IBGain-2^16) / 2^15

Otherwise, GainI2=IBGain / 2^15

Before calibration, I2a; after calibration, I2b. The relationship between them is: I2b=I2a + I2a × GainI2

Custom power registers D2FPL/D2FPH/D2FP2L/D2FP2H (0x11~0x12/0x65H~0x66H)

The custom power registers are 32-bit signed numbers, consisting of two groups: D2FPH (0x12H)/D2FPL (0x11H) and D2FP2H (0x66H)/D2FP2L (0x65H). The high 16 bits (D2FPH/D2FP2H) and the low 16 bits (D2FPL/D2FP2L) are used, with the high bits of D2FPH/D2FP2H serving as the sign bits.

For instance, when the D2FMx register (bit5~4 of EMUCON2) is configured for custom power, the MKE101R automatically performs integration based on the pulse constant settings upon writing a power value into the custom power register. The accumulated electrical energy is stored in EnergyD (0x2BH) and EnergyD2 (0x2CH), while the integrated pulses are output through the QF pin.

The system requires users to first write D2FPH, then D2FPL, and finally D2FP to activate the function. This feature enables apparent energy measurement, with D2FP2 functioning similarly.

This register is not involved in the calculation of the checksum.

DC bias correction register (0x13~0x16)

The MKE101R introduces three new channels with 20-bit DC bias correction registers, designed for measurement applications that do not require high-pass filters. For detailed DC bias correction methods, refer to Chapter 4: DC Application Specifications.

Clock control register CLKCON (0x1A)

SYSTEM Control Register (CLKCON) Address: 0x1A H Default Value: 0000H		
bit	**Position Name**	**functional description**
[15:4]	continue to have	Default is 0

3	PSM1_clk_en	Clock gating of synchronous sampling module 1. When the leakage detection mode pin MD0 is high (i.e., in fast-response mode), the default clock is enabled. After configuring the CLKCON register, the clock enable is controlled by the register. 2. When the leakage detection mode pin MD0 is low (i.e., in normal measurement mode), the default clock is disabled.
2	IIC_clk_en	IIC Clock gating 0: Close 1: Open
1	HSTX_clk_en	HSTX Clock gating 0: Close 1: Open
0	SWAVE_CLK_EN	Enable the waveform buffer module clock 0: Close 1: Open

Measurement Control Register 3 (0x60)

Energy Measure Control Register3 (EMUCON3) Address: 0x60 H Default Value: 0000H Bytes: 2		
bit	**Position Name**	**functional description**
15	start_cfg3	Comparison of Start-up Potential of D2F5/6/9 =0: The energy integration starts when the input power of the integrator exceeds the threshold. =1: The energy integration is activated when either the input power of this integrator or the input power of the paired integrator exceeds the threshold. A typical application is initiating metering when active or reactive power surpasses the threshold, effectively using the effective value of the current as the activation threshold. D2F5 (active power) and D2F6 (reactive power) form a pair, while D2F6 (reactive power) and D2F9 (fundamental active power) form another pair.
14	start_cfg2	Comparison of Start-up Potential of D2F3/4/8 =0: Starts the energy integration when the integrators input power exceeds the threshold. =1: The energy integration is activated when either the input power of this integrator or the input power of the paired integrator exceeds the threshold. A typical application is initiating metering when active or reactive power surpasses the threshold, effectively using the effective value of the current as the activation threshold. D2F3 (active power) and D2F4 (reactive power) form a pair, while D2F4 (reactive power) and D2F8 (fundamental active power) form another pair.

13	start_cfg1	Comparison of the Start-up Potential of D2F1/2/7 =0: The energy integration starts when the input power of the integrator exceeds the threshold. For example, if D2F1 is set to active power, the energy integration will start when the active power exceeds the threshold. =1: The energy integration is activated when either the input power of this integrator or the input power of the paired integrator exceeds the threshold. A typical application is initiating metering when active or reactive power surpasses the threshold, effectively using the effective value of the current as the activation threshold. D2F1 (active power) and D2F2 (reactive power) form a pair, while D2F2 (reactive power) and D2F7 (fundamental active power) form another pair.
[12:8]	cf_time[4:0]	This parameter defines the high-level pulse width for power pulse configuration. The 18-bit counter controls the pulse width, with a clock frequency of Fosc/2. The target count value is {cf_time[4:0],13 h0}, and the pulse transitions from high to low when the counter exceeds this value. When cf_time=0, the default target count is {5 h13H,13 h0}=18 h26000, with a typical pulse width of 87ms@Fosc3.579545MHz.
[7:6]	q2sum_mode[1:0]	In single-phase three-wire operation, when the input of D2F is set to q1+q2, the register determines the sign of the q1+q2 operation. For q2, it can be set to its original value, inverted, or cleared to zero during the addition process. =2b00: When two reactive power sources are combined, q2 is set to its original value =2b01: When adding two reactive power components, q2 is set to the inverted value =Other: When the two reactive power paths are combined, q2=0
[5:4]	q1sum_mode[1:0]	In single-phase three-wire operation, when the input of D2F is set to q1+q2, the register determines the sign of the q1+q2 operation. For q1 during addition, it can be set to original value, inverted, or reset to zero. =2b00: When two reactive power paths are combined, q1 is set to its original value =2b01: When two reactive power sources are summed, q1 is set to the inverted value =Other: When the two reactive power paths are combined, q1=0
[3:2]	p2sum_mode[1:0]	In single-phase three-wire operation, when the input of D2F is set to p1+p2, the register determines the sign of the p1+p2 operation. For p2, it can be set to its original value, inverted, or cleared to zero during the addition process. =2b00: When two active channels are summed, p2 is set to the original value

		=2b01: When summing two active signals, p2 is set to the inverted value =Other: When the two active paths are summed, p2=0
[1:0]	p1sum_mode[1:0]	In single-phase three-wire operation, when the input of D2F is set to p1+p2, the register determines the sign of the p1+p2 operation. For p1, it can be set to its original value, inverted, or reset to zero during the addition process. =2b00: When two active channels are summed, p1 is set to the original value =2b01: When summing two active signals, p1 is set to the inverted value =Other: When the two active paths are summed, p1=0

Measurement Control Register 4 (0x61)

Energy Measure Control Register4 (EMUCON4) Address: 0x61 H Default Value: 0000H Bytes: 2		
bit	**Position Name**	**functional description**
[15:14]	pmode6[1:0]	Control of the Integration Mode of D2F6 Integrator Define the same as pmode3
[13:12]	pmode5[1:0]	Control of the Integration Mode of D2F5 Integrator Define the same as pmode3
[11:10]	pmode4[1:0]	Control of the Integration Mode of D2F4 Integrator Define the same as pmode3
[9:8]	pmode3[1:0]	Control of the Integration Mode of D2F3 Integrator =2b00: Algebraic summation method, where Pfcnt3 is incremented during forward power and decremented during reverse power; =2b01: Forward power mode, where the forward power equals Pfcnt3 plus the reverse power, and the reverse power is not integrated. =2b10: Absolute value method, Pfcnt3 is added regardless of forward or reverse power; =2b11: Reverse power mode. During reverse power operation, Pfcnt3 is subtracted, while forward power does not participate in the integration.
7	frmsi_os_en	=0: IBRMSOS (0x0F) is used as the valid offset register for the IB channel; =1: IBRMSOS (0x0F) is used as the RMS offset register for the fundamental current channel;
[6:0]	Prun9~prun3	Prun9~prun3 controls whether the power integrators D2F9~D2F3 are enabled. =0: Do not enable integration =1: Enable integral

Measurement Control Register 5 (0x62)

Energy Measure Control Register4 (EMUCON5) Address: 0x62 H Default Value: 0000H Bytes: 2		
bit	**Position Name**	**functional description**
15	udc_off	=0: Enables U-channel DC offset correction in the measurement channel. The correction activates when the DC offset register is non-zero. =1: The U-channel in the measurement channel is disabled for DC offset correction, regardless of whether the register is zero.
14	iadc_off	=0: The IA channels measurement path activates DC offset correction. This correction applies when the DC offset register is non-zero. =1: The DC offset correction for the metering channels Ia path is disabled, and the correction will not apply regardless of whether the register is zero;
13	ibdc_off	=0: Enables DC offset correction on the IB channel of the measurement path. The correction activates when the DC offset register is not zero. =1: The DC offset correction for the IB channel in the measurement path is disabled, regardless of whether the register is zero.
12	IRQ_REV	=0: The IRQ pin is set to the default output level; =1: Output after inverting the IRQ pin level
11	QF_REV	=0: The QF pin is the default output level; =1: Invert the QF pin level and output
10	PF_REV	=0: The PF pin is the default output level; =1: Invert the PF pin level and output
[9:8]	d2fm6[1:0]	=00: The D2F6 power integration unit is configured to input reactive power, which is controlled by a dedicated channel selection command. By default, it uses channel As reactive power. =01: The input of the D2F6 power integration unit is set to D2FP2 custom power; =10: The input of the D2F6 energy integration unit is set to channel B reactive power; =11: The input of the D2F6 power integration unit is the vector sum of reactive power from channels A and B;
[7:6]	d2fm5[1:0]	The input selection for the D2F5 power integration unit is defined as the same as d2fm1.
[5:4]	d2fm4[1:0]	=00: The D2F4 energy integration unit is configured to input reactive power, which is controlled by a dedicated channel selection command. By default, it uses channel As reactive power.

		=01: The input of the D2F4 power integration unit is set to D2FP custom power; =10: The input selection for the D2F4 energy integration unit is reactive power from channel B; =11: The input of the D2F4 power integration unit is the vector sum of reactive power from channels A and B;
[3:2]	d2fm3[1:0]	The input selection for the D2F3 power integration unit is defined as the same as d2fm1.
[1:0]	d2fm1[1:0]	=00: The input of the D2F1 power integration unit is set to active power, which is controlled by a channel selection command. By default, it uses the active power from channel A. =01: The input of the D2F1 energy integration unit is set to channel A active power; =10: The input selection for the D2F1 energy integration unit is active power from channel B; =11: The input of the D2F1 power integration unit is the vector sum of active power from channels A and B;

Measurement Control Register 6 (0x63)

Energy Measure Control Register4 (EMUCON6) Address: 0x63 H Default Value: 0000H Bytes: 2		
bit	**Position Name**	**functional description**
15	qsel	Select position for full-wave reactive power and fundamental reactive power: =0: The reactive voltage is set to the full-wave voltage with a 90-degree phase shift, ensuring backward compatibility with other MKE101R series chip variants. This configuration enables simultaneous acquisition of both A and B reactive power values. =1: Reactive voltage is set to the fundamental voltage shifted 90 degrees, measuring only the fundamental reactive power. With this option, only one reactive power value is available.
[14:13]	splf_mode[1:0]	=00: SPL_FU (0x7C) outputs the instantaneous sampling waveform of the fundamental voltage, while SPL_FI (0x7D) outputs the instantaneous sampling waveform of the fundamental current. The update rate is 13.982 kHz at 3.579545 MHz. The high 3 bytes of the 4-byte data are valid, and the low byte is fixed to 0. =01: Sampling values at two points before and after the positive zero-crossing of the fundamental voltage output per cycle, along with the sampling points count of the preceding cycle. Specifically: SPL_FI[31:8] represents the value at the sampling point before the positive zero-crossing, SPL_FU[31:8] represents the value at the sampling point after the positive

		zero-crossing, and {SPL_FU[7:0], SPL_FI[7:0]} indicates the sampling points count of the cycle preceding the zero-crossing. =10: After the special zero-crossing count command (0xea, 0x7c) is activated, record the two sampling values before and after the first zero-crossing point following the command, as defined in 01. =11: Keep
12	flpf_selI	=0: The fundamental frequency measurement channel selects channel A; =1: The fundamental frequency measurement channel is set to channel B;
[11:10]	d2fm9[1:0]	=00: The input selection for the D2F9 energy integration unit is set to fundamental active power, controlled by flpf_selI. By default, it uses channel As fundamental active power. When selecting fundamental measurement, the G FS register must also be configured. For details, refer to the G FS register description. =01: The D2F9 power integration unit selects D2FP2 as its custom power input. =Other values: Keep;
[9:8]	d2fm8[1:0]	=00: The input selection for the D2F8 energy integration unit is set to fundamental active power, controlled by flpf_selI. By default, it uses channel As fundamental active power. When selecting fundamental measurement, the G FS register must also be configured. For details, refer to the G FS register description. =01: The D2F8 power integration unit is configured with the custom power input D2FP. =Other values: Keep;
[7:6]	d2fm7[1:0]	=00: The input for the D2F7 energy integration unit is set to fundamental active power, controlled by flpf_selI. By default, it uses channel As fundamental active power. When selecting fundamental measurement, the G FS register must also be configured. For details, see the G FS register description. =01: The D2F7 power integration unit is configured to use the custom power input D2FP. =Other values: Keep;
[5:4]	pmode9[1:0]	Corresponding to the power pulse integration unit D2F9, defined as pmode7[1:0]
[3:2]	pmode8[1:0]	Corresponding to the power pulse integration unit D2F8, defined as pmode7[1:0]
[1:0]	pmode7[1:0]	Corresponding to the electric energy pulse integration unit D2F7. Control the integration method of the D2F7 integrator. =2b00: Algebraic summation method, where Pfcnt7 is incremented during forward power and decremented during reverse power;

		=2b01: Forward power mode, where the forward power equals Pfcnt7 plus, and the reverse power is not integrated. =2b10: Absolute value method, Pfcnt7 is added regardless of forward or reverse power; =2b11: Reverse power mode. During reverse power operation, Pfcnt7 is subtracted, while forward power does not participate in the integration.

Pin Function Control Register (0x64)

PIN Control Register4 (PINCFG) Address: 0x64 H Default Value: 0000H Bytes: 2		
bit	**Position Name**	**functional description**
[15:12]	---	continue to have
[11:8]	PINCFG[11:8]	When IBDET_CFG.IB_Trigo_en=0, the output of the IRQ/ZX pin is determined by the following configuration: =4'h0：IRQ output IRQ =4h1: IRQ output CF2 (default QF) =4'h2：IRQ output CF3 =4'h3：IRQ output CF4 =4'h4：IRQ output CF5 =4'h5：IRQ output CF6 =4'h6：IRQ output CF7 =4'h7：IRQ output CF8 =4'h8：IRQ output CF9 =4h9: IRQ outputs IBTH (Input/Output Threshold Comparison) =4hA: IRQ output REVP (Negative Power Indicator) =4hB: IRQ output CF1 (i.e., the default PF) =4hC: IRQ output ZX (zero-crossing output) =4hD: IRQ output HSTX (high-speed UART port) =4hE: IRQ is selected as SCL =4hF: IRQ is set to SDA When IBDET_CFG.IB_Trigo_en=1, the IRQ/ZX pin is configured for IB_Trig functionality.
[7:4]	PINCFG[7:4]	=4h0: QF outputs CF2 (default QF) =4h1: QF outputs CF1 (default PF) =4'h2：QF output CF3 =4'h3：QF output CF4 =4'h4：QF output CF5 =4'h5：QF output CF6 =4'h6：QF output CF7 =4'h7：QF output CF8 =4'h8：QF output CF9 =4h9: QF outputs IBTH (Input/Output Threshold Comparison) =4hA: QF outputs REVP (negative work indication)

		=4hB: QF outputs IRQ (interrupt request) =4hC: QF outputs ZX (zero-crossing output) =4hD: QF outputs to HSTX (high-speed UART port) =4hE: Select SCL =4hF: Select SDA
[3:0]	PINCFG[3:0]	=4h0: PF outputs CF1 (default PF) =4h1: PF outputs CF2 (default QF) =4'h2：PF output CF3 =4'h3：PF output CF4 =4'h4：PF output CF5 =4'h5：PF output CF6 =4'h6：PF output CF7 =4'h7：PF output CF8 =4'h8：PF output CF9 =4h9: PF outputs IBTH (Input/Output Threshold Comparison for IB channel) =4hA: PF output REVP (Negative Work Indicator) =4hB: PF output IRQ (interrupt output) =4hC: PF output ZX (zero-crossing output) =4hD: PF outputs to HSTX (high-speed UART port) =4hE: Select SCL =4hF: Select SDA

Active power phase compensation registers PPhsCalA/PPhsCalB (0x67/0x68)

Reactive Power Phase Calibration Register (PPhsCalA)			Address: 67H		Default Value : 0000H		
	Bit15	14	13	12..3	2	1	Bit0
Read: / Write:	PPC15	PPC14	PPC13	PPC12 QPC3	PPC2	PPC1	PPC0
Reset:	0	0	0	0 0	0	0	0

Reactive Power Phase Calibration Register (PPhsCalB)			Address: 68H		Default Value : 0000H		
	Bit15	14	13	12..3	2	1	Bit0
Read: / Write:	PPC15	PPC14	PPC13	PPC12 QPC3	PPC2	PPC1	PPC0
Reset:	0	0	0	0 0	0	0	0

The active power phase compensation register is designed to perform phase compensation for active power. Unlike channel phase compensation (0x07~0x08), it offers finer calibration and a wider range. The register employs a 16-bit binary complement format, with the most significant bit (MSB) serving as the sign bit. For operational instructions, refer to Chapter 3: Meter Calibration Methods.

Correction formula: P2 = P1-PPhs * Q1

Where Q1 is the reactive power, P1 is the active power before compensation, and P2 is the active power after compensation.

Half-wave power and half-wave RMS control register HWCFG (0x69)

HW Control Register (HWCFG) Address: 0x69 H Default Value: 0000H Bytes: 2		
bit	**Position Name**	**functional description**
15	hw_zx_sel	The Selection of Zero Crossing Signal in Half Power or Half Effective Value Calculation =1: Select full-wave zero-crossing =0: Select zero-crossing for the fundamental wave. It is recommended to choose zero-crossing for the fundamental wave.
14	qbhw_d2f_sel	The 100Hz low-pass filter (LPF1) for B-channel reactive power metering can be disabled. =1: Turn off the LPF1 of the QB channel =0: Enable LPF1 for the QB channel
13	pbhw_d2f_sel	The 100Hz low-pass filter (LPF1) for the B-phase active power metering can be disabled. =1: Turn off LPF1 for the PB channel =0: Enable LPF1 for the PB channel
12	qahw_d2f_sel	Selection of Half-wave Power Metering for Reactive Power in A Line =1: For A line reactive power metering, half-wave power is used for energy calculation; =0: For the A line reactive power, the instantaneous power after selecting LPF1 is used for energy calculation;
11	pahw_d2f_sel	Selection of Active Power Half-wave Power Metering for A Line =1: For active power measurement on line A, half-wave power is used for energy calculation. =0: For the active power of circuit A, the instantaneous power after selecting LPF1 is used for power calculation;
10	hw_qa_mode	Selection of Half-wave Measurement Method for Reactive Power in A Line =1: For the A channel, the reactive power is calculated using the zero-crossing method by summing the instantaneous power values between two zero-crossing points and dividing by the number of sampling points between these points. =0: For A channel, the reactive power is calculated by accumulating the half-wave values of fixed-point numbers, i.e., the instantaneous power values of the fixed-point numbers are accumulated and then divided by the fixed-point number.
9	hw_pa_mode	The Selection of Half-wave Measurement Method for Active Power of A Line (Including Full-wave Active Power and Fundamental Active Power) =1: For the A channel, the active power is calculated using the

		zero-crossing method by summing the instantaneous power values between two zero-crossing points and dividing by the number of sampling points between these points. =0: For the A channel, the active power is calculated by accumulating the half-wave values of fixed-point numbers, i.e., the instantaneous power values of the fixed-point numbers are accumulated and then divided by the fixed-point number.
[8:0]	hw_num[8:0]	When the half-cycle updated power or RMS value is calculated using a fixed number of points, this register sets the number of calculation points. = 9b0, calculated by averaging 140 points over half a cycle; = 9b1, calculated by averaging 1-point accumulations over half a cycle; = 9b1x, calculated by averaging the 2-point accumulation over half a cycle; = 9b1xx, calculated by averaging the 4-point semi-period accumulation; = 9b1xxx, calculated by averaging the 8-point semi-period accumulation; = 9b1xxxx, calculated by averaging 16-point accumulations over half a cycle; = 9b1xxxxx, calculated by averaging 32 points over half a cycle; = 0x40~0x1FF. If the target half-period cumulative average count is N, set hw_num to N.

Synchronous sampling channel control register 1 SWAVECFG1 (0x6B)

SWAVE Control Register1 (SWAVECFG1) Address: 0x6B H Default Value: 0000H Bytes: 2		
bit	**Position Name**	**functional description**
[15:10]	**continue to have**	**continue to have**
9:8	swave_div[1:0]	Determine the frequency division coefficient when synchronizing the sampling waveform output. =2b00: No frequency division =2b01:2-fold split =2b10:4-fold frequency division =2b11:8-bit split For instance, when the SWAVECFG2 register sets the synchronous sampling points to 256, the typical sampling rate is F*256. If wave_div[1:0]=2b01, the final output waveform will have a sampling rate of F*256/2.
7	swave_p_en	=0: The HW_PA (0x4DH) register outputs the half-wave power

		calculated by the synchronous sampling channel, with its theoretical value equal to PowerPA (0x26). =1: HW_PA (0x4DH) outputs the half-wave power calculated by the metering channel. The theoretical value of this register equals PowerPA (0x26).
6	Swave_out_en	=0: The waveform register (0x30/0x31/0x32) outputs 14KHz data at a fixed sampling rate, with 20 bits of valid data and the most significant bit as the sign bit. =1: The waveform register (0x30/0x31/0x32) outputs synchronous sampling data with a sampling rate automatically adjusted according to the power frequency. It has 24 valid bits, and the most significant bit is the sign bit.
5	Aac_off	AAC calibration primarily compensates for the gain of harmonics in the synchronous sampling channel, which compensates for the harmonic attenuation caused by the CIC comb filter commonly used in sigma-delta ADCs, ensuring that the gain error of all harmonics within the bandwidth remains essentially consistent. =0: Enable AAC correction for the synchronized sampling channel; =1: Disable AAC correction for the sync sampling channel;
4	Agc_off	The AGC correction compensates the difference of fixed gain of CIC filter caused by different sampling rates in the synchronous sampling channel, and ensures the same gain value at different sampling rates. =0: Enable AGC correction for the synchronized sampling channel; =1: Disable AGC correction for the synchronized sampling channel;
3	Swave_dc_en	=0: Disable DC offset correction for the synchronous sampling channel; =1: Enable DC offset correction for the synchronous sampling channel; The registers 0x13~0x16 will only affect the synchronous sampling channel when DC offset correction is enabled.
2	Swave_hpfu_on	=0: Turn off the high-pass filter for the U channel in synchronous sampling; =1: Enable the high-pass filter for the U channel in synchronous sampling;
1	Swave_hpfib_on	=0: Turn off the high-pass filter for the IB sampling channel; =1: Enable the high-pass filter for the synchronous sampling channel IB;
0	Swave_hpfia_on	=0: Turn off the high-pass filter for the Ia channel; =1: Enable the high-pass filter for the I/A channel in

		synchronous sampling mode;

The synchronous sampling channel control register 2 SWAVECFG2 (0x6C)

SWAVE Control Register2 (SWAVECFG2) Address: 0x6C H Default Value: 0000H Bytes: 2		
bit	**Position Name**	**functional description**
[15:13]	swave_hw[2:0]	The wave_hw[2:0] determines the accumulation points for both the half-wave RMS value (at addresses 0x4F/0x77/0x78) and the half-wave power of the synchronous sampling channel, as defined below: swave_hw[2:0]=3b000:128-point accumulation swave_hw[2:0]=3b001:64-point accumulation swave_hw[2:0]=3b010:32-point accumulation swave_hw[2:0]=3b011:256-point accumulation swave_hw[2:0]=3b100:512-point accumulation swave_hw[2:0]=3b101:1024-point accumulation swave_hw[2:0]=Other values: retained The cumulative number of points and the number of synchronous sampling points need to be set independently. For example, if the synchronous sampling is set to 256 points per cycle, the cumulative points for half-wave RMS value should be at least 128 (typically updated every 10ms) or 256 (typically updated every 20ms). Setting it to 64 points will result in incorrect RMS values.
[12:10]	swavecfg[2:0]	When wavecnt[9:0]=0, hardware adaptive synchronous sampling is implemented. The hardware automatically adjusts the sampling rate according to power frequency variations to meet the required sampling points, which are defined by wavecfg. Swavecfg[2:0]=3b000: Synchronous sampling at 256 points per week Swavecfg[2:0]=3b001: Synchronous sampling at 128 points per week Swavecfg[2:0]=3b010:64-point weekly wave synchronization sampling Swavecfg[2:0]=3b011: Synchronous sampling at 512 points per week Swavecfg[2:0]=3b100:10 cycles 1024-point synchronous sampling Swavecfg[2:0]=3b101:10 frequency 2048-point synchronous sampling Swavecfg[2:0]=Other: Keep When wavecnt[9:0]=0, the number of sampling points is determined by wavecnt. The final sampling rate is: fosc/2/(wavecnt+1)
[9:0]	wavecnt[9:0]	

Synchronous sampling channel phase correction register Swave_PHSIA/PHSIB/PHSU (0x6D/0x6E/0x6F)

address	name	read-write	byte	Windows default	function declaration
6DH	Swave_PHSIA	R/W	2	0000h	Phase Correction of Synchronous Sampling Channel IA
6EH	Swave_PHSIB	R/W	2	0000h	Phase Correction of Synchronous Sampling Channel IB
6FH	Swave_PHSU	R/W	2	0000h	Phase Correction of Synchronous Sampling Channel U

The three phase correction registers of the synchronous sampling channel are all operated in 2 bytes, with an actual effective bit depth of 7 bits.

Each scale represents a phase shift delay of 360 degrees/(fosc/2/F), as illustrated below:

At 50Hz, the phase shift scale is calculated as: 360 degrees/(3579545/2/50) =0.010057 degrees.

The maximum phase shift is 128 times of the phase shift scale.

Synchronous sampling channel gain correction register (0x70/0x71/0x72)

address	name	read-write	byte	Windows default	function declaration
70H	Swave_GSIA	R/W	2	0000h	Gain Correction of Synchronous Sampling Channel IA
71H	Swave_GSIB	R/W	2	0000h	Gain Correction of Synchronous Sampling Channel IB
72H	Swave_GSU	R/W	2	0000h	Gain Correction of Synchronous Sampling Channel U

It includes three registers in binary complement format, with the most significant bit as the sign bit. These registers are used for gain correction of three synchronous sampling channels.

The correction formula is: Swave1=Swave0 × (1 + GS)

The GS is the normalized value of gain correction register, which is in the range of ±1.

Fundamental Power Gain Correction Register (GFP) (0x73)

address	name	read-write	byte	Windows default	function declaration
73H	GFP	R/W	2	0000h	fundamental active power gain correction register

GFP is a binary complement format with the most significant bit as the sign bit. It is used for gain correction of fundamental active power.

The correction formula is: FP1=FP0 (1 + GFP)

Here, GFP is the normalized value of the gain correction register, with a range of ±1.

Fundamental power active power offset correction register FPOS (0x74)

addr	name	read	byte	Windows	function declaration

ess		-writ e		default	
74H	FPOS	R/W	2	0000h	fundamental active power offset correction register

The fundamental power offset correction is designed for precision adjustment of small signals. This register uses binary complement format, with the most significant bit as the sign bit. Its usage is identical to the power offset correction registers APOSA and APOSB.

IB Half-Wave Effective Value Threshold Register IBTH (0x75)

addr ess	name	read -writ e	byte	Windows default	function declaration
75H	IBTH	R/W	2	0000h	The IB channel half-wave RMS threshold register is a 16-bit register. The 16-bit high of the half-wave RMS value HW_IB[23:0] is compared with the register {IBTH[15:2],2h0}. When HW_IB exceeds the threshold, its value is cached in the 0x76H register (HW_IBTH), and a read-clear flag signal IBTH_FLAG is generated in the 0x31H register (extended register IBDET_FLG), which can also be output to external pins. When IBTH[15:2] equals 0, the IBTH threshold defaults to 0x147. IBTH[1:0] determines the number of half-periods exceeding the threshold. =2b00: Exceeds the threshold once; =2b01: Two times exceeded the threshold; =2b10: Exceeds the threshold three times; =2b11: Exceeded the threshold four times.

Fundamental Voltage and Current Gain Register (GFS) (0x5E)

addr ess	name	read -writ e	byte	Windows default	function declaration

5EH	GFS	R/W	2	0000h	The gain register for fundamental voltage and current. When this register is set to 0, the system defaults to using internal hardware gain compensation, which primarily compensates for the attenuation of the fundamental filter in 60Hz applications. If the register is not set to 0, it serves as the gain compensation value, with the software specifying the compensation value. The register is in twos complement format. The correction formula is: F2=F1 × (1 + GFS), where GFS is a normalized value ranging from-1 to 1, F1 is the pre-correction fundamental wave sampling value, and F2 is the post-correction fundamental wave sampling value. **Note: The recommended configuration is 0x0 @3.579545MHz and 0xFFE8@5.5296MHz.**

2.1 5.3 Measurement Parameter Registers

Fast Pulse Counter PFCNT/DFCNT (0x20/0x21)

Active Energy Counter Register (PFCNT)				Address: 0x20h			
	Bit15	14	13	12 … 3	2	1	Bit0
Read: / Write:	PFC15	PFC14	PFC13	PFC12…PFC3	PFC2	PFC1	PFC0
Reset:	0	0	0	0	0	0	0

Reactive Energy Counter Register (DFCNT)				Address： 0x21h			
	Bit15	14	13	12 … 3	2	1	Bit0
Read: / Write:	QFC15	QFC14	QFC13	QFC12…QFC3	QFC2	QFC1	QFC0
Reset:	0	0	0	0	0	0	0

To prevent power loss during power-on and power-off cycles, the MCU can read back and store the values of registers PFCnt/DFcnt during a power outage, then rewrite these values into PFCnt/DFcnt upon the next power-on.

When the absolute value of the count value in the fast pulse counting register PFCnt/DFcnt is twice or greater than HFconst, the corresponding PF/QF will experience pulse overflow, and the energy register value will be incremented by 1 accordingly.

Assuming the pulse constant of the meter is EC, one pulse of PF/QF represents 1/EC of energy, and the minimum scale of PFcnt/DFcnt represents 1/(EC*HFconst*2) of energy.

Current Voltage RMS Registers IARMS/IBRMS/URMS (0x22/0x23/0x24)

Current A Rms Register (IARms)			Address：0x22h				
	Bit23	22	21	20 … 3	2	1	Bit0
Read:	IAS23	IAS22	IAS21	IAS20…IAS3	IAS2	IAS1	IAS0

Current B Rms Register (IBRms)			Address：0x23h				
	Bit23	22	21	20 … 3	2	1	Bit0
Read:	IBS23	IBS22	IBS21	IBS20…IBS3	IBS2	IBS1	IBS0

Voltage Rms Register (Urms)			Address：0x24h				
	Bit23	22	21	20 … 3	2	1	Bit0
Read:	US23	US22	US21	US20…US3	US2	US1	US0

The RMS valid value is a three-byte register. BIT[22:0] contains the valid data, while BIT[23] is a data validity flag: 0 indicates valid data, and 1 indicates invalid data, which will be discarded.
The relationship between the measured signal voltage and the valid value register and the input pin of the chip:

Rms = (Vpn×PGA÷1000)×2^23

Rms: The register value of the RMS.

Vpn: The voltage between the positive and negative analog input pins of the corresponding measurement channel, measured in millivolts.

PGA: Gain amplification factor of the corresponding measurement channel.

In the equation, 1000 indicates the maximum input signal for normal pin operation: ±1000mV. Note that the effective value of AC current must be considered. $\sqrt{The\ maximum\ value\ (2)\ is\ less\ than\ 1000\ mV}$.

In the equation, 2^23 indicates that the maximum register value is 2^23 = 8388608 when Vpp is 1000mV.

For example, the voltage between pins V1P and V2P is 1mV. With the IA channel PGA configured at 16x, the IARms value is calculated as (1 × 16 ÷ 1000) × 2^23 = 134217.728, corresponding to the register value 0x0 20C49.

Note: The lower three bits of the register serve as flag bits, where bit[0] is fixed at 1, and bit[2:0] cycles through the values 00 1-01 1-10 1-11 1.

The default update frequency for valid parameters is 3.414H z@F osc 3.579545MHz or 5.27 Hz@Fosc 5.5296 MHz. Other update frequencies can be configured as detailed in the EMUCON2.UPMODE description.

Voltage frequency register UFreq (0x25)

Voltage Frequency Register (UFreq)			Address：0x25h				
	Bit15	14	13	12 … 3	2	1	Bit0
Read:	Ufreq15	Ufreq14	Ufreq13	Ufreq12…Ufreq3	Ufreq2	Ufreq1	Ufreq0

1. Frequency Measurement Characteristics

-Measured quantity: fundamental frequency

-Bandwidth measurement: ≈250Hz

-Data format: 16-bit unsigned integer

2. Frequency Calculation Formula

f = (CLKIN × n) / (256 × UFREQ)

among ：

-CLKIN: Clock frequency of the metering chip system (Hz)

-n: The update cycle for frequency measurement configured by EMUCON2.FreqCnt, measured in power grid cycles (default: 32 cycles)

-UFREQ: Voltage frequency register UFreq (0x25)

3. Example calculation

When the parameter is:

CLKIN = 3.579545MHz

n = 32

UFREQ = 8948

Measured frequency:

f = (3579545 × 32)/(256 × 8948) ≈ 49.9908Hz

4. Description of Registers

-Update cycle: Default 0.64 seconds (50Hz grid, 32 Hz update by default; adjustable via Metering Control Register 2, EMUCON2.FreqCnt)

-UFreq (0x25H): Frequency register

-UFreq2 (0x35H): Frequency register 2, 3-byte word length, calculated as UFreq

Average active power registers PowerPA/PowerPB (0x26/0x27)

Active Power Register (PowerPA)			Address：0x26h				
	Bit31	30	29	28 … 3	2	1	Bit0
Read:	APA31	APA30	APA29	APA28…APA3	APA2	APA1	APA0

Active Power Register (PowerPB)			Address：0x27h				
	Bit31	30	29	28 … 3	2	1	Bit0
Read:	APB31	APB30	APB29	APB28…APB3	APB2	APB1	APB0

The active power parameter PowerP is a 32-bit binary complement format, with the most significant bit being the sign bit. The default update frequency is 3.414H z@F osc 3.579545MHz or 5.27 Hz@Fosc 5.5296 MHz, but it can be configured for other frequencies. For details, refer to the EMUCON2.UPMODE description.

PowerPA is the average active power register for both U and I channels, while PowerPB is the corresponding average active power register for U and I channels.

The lowest three bits of the register are flag bits, where bit[0] is fixed to 1, and bit[2:0] cycles from 00 1 to 11 1.

Average reactive power registers PowerQ/PowerQB (0x28/0x36)

Reactive Power Register (PowerQ)			Address：0x28h				
	Bit31	30	29	28 … 3	2	1	Bit0
Read:	RP31	RP30	RP29	RP28…RP3	RP2	RP1	RP0

The reactive power parameter PowerQ is a 32-bit binary complement format, with the most significant bit as the sign bit. It updates at the same frequency as PowerPA and PowerPB. PowerQ represents the reactive power of channel A.

This register stores the reactive power calculation results for both U-channel and user-selected current channels, with channel A being the default selection.

The lower three bits of the register function as flag bits, where bit[0] is fixed at 1, and bit[2:0] cycles through the values 001,011,101, and 111 for updated data.

Reactive Power Register (PowerQB)			Address：0x36h				
	Bit31	30	29	28 … 3	2	1	Bit0
Read:	RP31	RP30	RP29	RP28…RP3	RP2	RP1	RP0

The reactive power parameter PowerQB is a 32-bit binary complement format, with the most significant bit being the sign bit. It updates at the same frequency as PowerPA and PowerPB. PowerQB represents the reactive power of channel B.

The lower three bits of the register function as flag bits, where bit[0] is fixed to 1, and bit[2:0] cycles through the values 001,011,101, and 111 for updated data.

Active energy registers EnergyP/ EnergyP2 (0x29/0x2A)

Active Energy Register (EnergyP)			Address：0x29h				
	Bit23	22	21	20 … 3	2	1	Bit0
Read:	EP23	EP22	EP21	EP20…EP3	EP2	EP1	EP0

The EnergyP register is an accumulator or reset-type functional register. When configured as an accumulator (bit15 of the EMUCON register set to 0), the PEOIF overflow flag is generated when 0xFFFFFF overflows to 0x000000 (see IF 0x41H). When configured as a reset-type (bit15 of the EMUCON register set to 1), the register is reset to 0 after reading.

Energy parameters are unsigned numbers. The register values of EnergyP represent the cumulative count of PF pulses. The smallest unit of energy in the register is 1/EC kWh, where EC is the meter constant.

Active Energy Register2 (EnergyP2)			Address：0x2AH				
	Bit23	22	21	20 … 3	2	1	Bit0
Read:	EP23_2	EP22_2	EP21_2	EP20_2…EP3_2	EP2_2	EP1_2	EP0_2

When the energy_fz bit in metering control register 2 is 0, it functions as a read-only active power register. When the energy_fz bit is 1, the register activates its timed freeze function, periodically loading the active power register (address 29) with its value every 2048×1024×Fosc cycles (572.1397 ms@3.579545 MHz), while simultaneously resetting the active power register.

Reactive or custom energy registers EnergyD/EnergyD2 (0x2B~0x2C)

UserDEIFNE Energy Register (EnergyD)			Address：0x2BH				
	Bit23	22	21	20 … 3	2	1	Bit0
Read:	EP23	EP22	EP21	EP20…EP3	EP2	EP1	EP0

The EnergyD register is an accumulator-type custom energy register. When configured as an accumulator (EMUCON register bit15=0), it generates an overflow flag QEOIF (see IF 0x41H) when 0xFFFFFF overflows to 0x000000. When configured as a reset type (EMUCON register bit15=1), the register resets to 0 after reading.

EnergyD registers store unsigned energy parameters, each representing the cumulative count of QF pulses. The registers smallest unit equals 1/EC kVARh, where EC is the energy constant.

EnergyD is the default reactive power register. It can be configured using the EMUCON2 register.

UserDEFINE Energy Register2 (EnergyD2)			Address：0x2CH				
	Bit23	22	21	20 … 3	2	1	Bit0
Read:	EP23_2	EP22_2	EP21_2	EP20_2…EP3_2	EP2_2	EP1_2	EP0_2

When the energy_fz bit in metering control register 2 is 0, it functions as a read-only resetable custom power register. When the energy_fz bit is 1, the register activates its timed freeze function, periodically loading the value from the custom power register (address 2B) into this register at 2048×1024×Fosc intervals (572.1397 ms@3.579545 MHz), while simultaneously resetting the custom power register.

EMUStatus/EMUStatus2/EMUStatus3 (0x2D/0x2E/0x2F)

This register includes two parts, the metering status register and the checksum register.

EMU STATUS Register (EMUStatus) Address: 0x2D Read-Only Register		
bit	**Position Name**	**functional description**
22	VREFLOW	Read-only register, indicating the VREF operating state. =1, indicating the REFV pin voltage is too low, suggesting an external circuit fault; =0, indicating that the REFV pin voltage has never been too low.
21	CHNSEL	Channel selection status flag. =1 indicates that channel B is currently used to calculate active power; =0 indicates that channel A is currently used to calculate active power. By default, this bit is set to 0, indicating channel A is selected for electricity metering.
20	Noqld	When the custom power is lower than the startup power, NoPld is set to 1; when the custom power is equal to or greater than the startup power, NoPLd is cleared to 0.

19	Nopld	When the active power is lower than the starting power, NoPld is set to 1; when the active power is equal to or greater than the starting power, NoPLd is cleared to 0.
18	REVQ	Reverse custom power indication signal: Set to 1 when negative power is detected, and to 0 when positive power is detected again. Update this value when the QF pulse is issued.
17	REVP	The reverse active power indicator signal is 1 when negative active power is detected and 0 when positive active power is detected again. This value is updated during the PF pulse.
16	ChksumBusy	The register of the status of the data check calculation of the meter. ChksumBusy =0, indicating the checksum calculation for the calibration table data is complete. The checksum value is available. ChksumBusy =1 indicates that the checksum calculation for the calibration table data is incomplete. The checksum value is unavailable.
15:0	Chksum	checksum output

EMU Status Register (EMUStatus2) Address: 0x2E Read-Only Register		
bit	**Position Name**	**functional description**
[23:8]	CRC	CRC[15:0]: The 16-bit CRC result from the metering configuration register.
7	CRCBusy	CRC data check calculation status register. CRCBusy =0 indicates that the CRC calculation for calibration data is complete. The checksum is available. CRCBusy =1 indicates that the CRC calculation for calibration data is incomplete. The checksum is unavailable.
6:4	----	The readout remains 0
3	HUFRMS_UP	The flag for updating the RMS value of the fundamental wave with half-cycle updates is cleared after reading. The RMS value calculated from the fundamental wave data updated by the metering channel.
2	HWRMS_UP	A half-cycle update flag for the full-wave RMS value, which is cleared after reading; the RMS value calculated from the full-wave data obtained from the synchronous sampling channel
1	BGR_OK	Read-only register, indicating the BGR operating state (Schmidt method) =1, indicating the BGR pin outputs a high voltage level; =0, indicating the BGR pin voltage is too low;
0	VREF_OK	Read-only register indicating the state of reference voltage VREF (comparator mode, current comparison) =1, indicating that the reference voltage VREF of the REFV pin output is normal; =0, indicating that the reference voltage VREF of the REFV pin output is too low;

EMU Status Register3 (EMUStatus3) Address: 0x2F, a 4-byte read-only register		
bit	**Position Name**	**functional description**
[31:22]	swave_time[9:0]	The read-only register indicates the actual frequency reduction ratio of the current synchronous sampling channel, which has the same meaning as wavecnt[9:0].
21	CF9	Corresponding to D2F9, with the same definition as CF3
20	CF8	Corresponding to D2F8, with the same definition as CF3
19	CF7	Corresponding to D2F7, with the same definition as CF3
18	CF6	Corresponding to D2F6, with the same definition as CF3
17	CF5	Corresponding to D2F5, with the same definition as CF3
16	CF4	Corresponding to D2F4, with the same definition as CF3
15	CF3	The CF3 pulse indication signal from the energy integration unit D2F3 is reset upon reading. A value of 1 indicates the generation of CF3 pulse, while 0 indicates no CF3 pulse is generated.
14	Nopld9	Corresponding to D2F9, with the same definition as Nopld3
13	Nopld8	Corresponding to D2F8, with the same definition as Nopld3
12	Nopld7	Corresponding to D2F7, with the same definition as Nopld3
11	Nopld6	Corresponding to D2F6, with the same definition as Nopld3
10	Nopld5	Corresponding to D2F5, with the same definition as Nopld3
9	Nopld4	Corresponding to D2F4, with the same definition as Nopld3
8	Nopld3	The latent start-up indicator signal of the electric energy integration unit D2F3 is a read-only bit: =1 indicates D2F3 is in the start-up state, while =0 indicates it is in the latent state.
7	REVP9	Corresponding to D2F9, with the same definition as REVP3
6	REVP8	Corresponding to D2F8, with the same definition as REVP3
5	REVP7	Corresponding to D2F7, with the same definition as REVP3
4	REVP6	Corresponding to D2F6, with the same definition as REVP3
3	REVP5	Corresponding to D2F5, with the same definition as REVP3
2	REVP4	Corresponding to D2F4, with the same definition as REVP3
1	REVP3	The reverse power indication signal of the energy integration unit D2F3 is a read-only bit: =1 indicates the current pulse is reverse, =0 indicates the current pulse is forward, and it is updated synchronously with the CF3 pulse.
0	continue to have	The readout has always been 1

Instantaneous sampling value registers SPL_IA/IB/U (0x30/0x31/0x32)

Register the instantaneous sampling value of the IAI (SPL_IA)		**Address: 0x30h**				
	Bit23~Bit20	**19**	**18 … 3**	**2**	**1**	**Bit0**
Read:	0	SPL_IA 19	SPL_IA 18…SPL_IA 3	SPL_IA 2	SPL_IA 1	SPL_IA 0

SPL_IA represents the instantaneous ADC sampling value after high-pass filtering for the IA

channel. It is a 20-bit signed number using twos complement format, with the high two bits as the sign bit. The data refresh rate is approximately F osc/2/128,2 1.6 kHz at 5.5296 MHz.

Register the SPL_IB for IB instant sampling values		Address: 0x31h				
	Bit23~Bit20	19	18 … 3	2	1	Bit0
Read:	0	SPL_IB 19	SPL_IB18…SPL_IB 3	SPL_IB2	SPL_IB 1	SPL_IB 0

SPL_IB represents the ADCs instantaneous sampling value after high-pass filtering in the IB channel. It is a 20-bit signed number using twos complement format, with the high two bits as the sign bit. The data refresh rate is approximately F osc/2/128,2 1.6 kHz at 5.5296 MHz.

U instantaneous sampling value Register SPL_U)		Address: 0x32h				
	Bit23~Bit20	19	18 … 3	2	1	Bit0
Read:	0	SPL_U 19	SPL_U 18…SPL_U 3	SPL_U 2	SPL_U 1	SPL_U 0

SPL_U represents the ADCs instantaneous sampling value after high-pass filtering in the U channel, with a 20-bit signed number using twos complement format (the high two bits being the sign bit). The data refresh rate is approximately F osc/2/128,2 1.6 kHz at 5.5296 MHz.

Zero Crossing Count Register ZXCNT (0x34)

ZX CNT Register (ZXCNT)			Address: 0x34h				
	Bit15	14	13	12 … 3	2	1	Bit0
Read:	ZXCNT 23	ZXCNT 22	ZXCNT 21	ZXCNT 20…ZXCNT 3	ZXCNT 2	ZXCNT 1	ZXCNT 0

When the software executes the zero-crossing measurement command (0xea/0x7c), the metering chip uses this commands timestamp as a reference point. It calculates the time difference between the voltages zero-crossing and this reference point, then stores the result in the ZXCNT (0x34H) register.

The register stores the time reference and the actual voltage zero-crossing time count, with a minimum unit of 256 crystal oscillator cycles, i.e., 71.517 μs@3.579545 MHz. After the special command is initiated, one cycle completes the measurement, and the measurement value remains unchanged until the next special command is issued.

Energy registers 3~9 (0x37~0x3D)

Energy Register (Energy3~9)			Address: 0x37h~0x3D				
	Bit23	22	21	20 … 3	2	1	Bit0
Read:	E23	E22	E21	E20…EP3	E2	E1	E0

Energy3~9 registers are functional registers with either accumulation or reset modes. When configured for accumulation (bit15 of EMUCON register set to 0), an overflow flag (PEOIF) is generated when 0xFFFFFF overflows to 0x000000 (see IF 0x41H). When configured for reset (bit15 of EMUCON register set to 1), the register is reset to 0 after reading.

Energy parameters are unsigned numbers. The values in registers Energy3~9 represent the cumulative count of CF3~CF9 pulses, corresponding to the D2F3~D2F9 energy pulse integration units. The minimum unit of energy in the register is 1/EC kWh, where EC is the meter constant.

Fast pulse counter Pfcnt3~9 (0x3E/3F,0x48~0x4C)

Energy Counter Register(Pfcnt3~9)			Address: 0x3E/3F,0x48~0x4C				
	Bit23	22	21	20 … 3	2	1	Bit0
Read:	PFC23	PFC22	PFC21	PFC20…PFC3	PFC2	PFC1	PFC0

Pfcnt3~9 correspond to the seven energy integration units D2F3~P2F9. The fast pulse counter counts the input pulses. When the absolute value of the pulse count in PFCnt doubles or exceeds HFconst, the corresponding CF will experience pulse overflow, and the energy register value will be incremented by 1.

Assuming the pulse constant of the meter is EC, one pulse of CF represents 1/EC of energy, while the minimum scale of PFcnt represents 1/(EC*HFconst*2) of energy.

Half-wave update of full-wave active power HW_PA (0x4D)

address	name	read-write	byte	Windows default	function declaration
4DH	HW_PA	R	4	00000000h	The half-cycle updated full-wave active power A, a 32-bit signed number in binary complement format, has a theoretical value identical to the PowerPA (0x26) register. This register has two output parameters, controlled by wave_p_sel. =0: HW_PA (0x4DH) outputs the half-wave power calculated by the synchronous sampling channel. The high-pass filter is disabled by default for faster dynamic response. =1: HW_PA (0x4DH) outputs the half-wave power calculated by the metering channel. High-pass filtering is enabled by default, which may increase response time due to the high-pass filter.

Half-wave reactive power update HW_PA (0x4E)

address	name	read-write	byte	Windows default	function declaration
4EH	HW_QA	R	4	00000000h	The full-wave reactive power A with half-cycle updates, derived from the half-wave reactive power calculated by the metering channel. This 32-bit signed binary complement register matches the theoretical value of the PowerQA (0x27) register.

Half-wave update effective value HW_IA/HW_IBTH/HW_IB/HW_U (0x4F/0x76/0x77/0x78)

address	name	read-write	byte	Windows default	function declaration
4FH	HW_IA	R	3	000000	The half-cycle update of the full-wave IARMS channels RMS value, a 24-bit unsigned number, has a theoretical value of 0.900316316*IARMS (0x22).
76H	HW_IBTH	R	3	000000	When the half-wave RMS value of the IB channel exceeds the threshold IBTH (0x75), its value HW_IB is cached in the register, a 24-bit unsigned number.
77H	HW_IB	R	3	000000	The half-cycle update of the full-wave IB channels effective value, a 24-bit unsigned number, has a theoretical value of 0.900316316*IBRMS (0x23).
78H	HW_U	R	3	000000	The RMS value of the full-wave U-channel with half-cycle updates, a 24-bit unsigned number, is theoretically calculated as 0.900316316*URMS (0x24).

The half-cycle update of the fundamental waves effective value, HW_FU/HW_FI (0x79/0x7A)

address	name	read-write	byte	Windows default	function declaration
79H	HW_FU	R	3	000000	The RMS value of the fundamental U-channel, updated semi-periodically, is a 24-bit unsigned number. When only the fundamental is present, its theoretical value equals URMS (0x24).
7AH	HW_FI	R	3	000000	The RMS value of the fundamental I channel with half-cycle updates, a 24-bit unsigned number, has the same theoretical value as IRMS (0x22 or 0x23) when only the fundamental is present.

Half-wave update of fundamental active power HW_FP (0x7B)

address	name	read-write	byte	Windows default	function declaration
7BH	HW_FP	R	4	000000	The half-cycle updated fundamental active power, a 32-bit signed number, has a theoretical value identical to PowerPA (0x26) when only the fundamental is present.

Half-cycle update of the fundamental instantaneous sampling value SPL_FU/SPL_FI (0x7C/0x7D)

addr	name	read	byte	Windows	function declaration

ess		-write		default	
7CH	SPL_FU	R	4	000000	Controlled by splf_mode[1:0], it outputs either the instantaneous sampling waveform of the fundamental wave or the voltage sampling data at two points before and after the zero-crossing. splf_mode[1:0] =00: SPL_FU outputs the instantaneous sampling waveform of the fundamental voltage, while SPL_FI outputs the instantaneous sampling waveform of the fundamental current. The update rate is F osc/2/128, with a frequency of 2 1.6 kHz at 5.5296 MHz. The high 3 bytes of the 4-byte data are valid, and the low byte is fixed to 0. =01: Sampling values at two points before and after the positive zero-crossing of the fundamental voltage in each cycle, along with the sampling points from the preceding cycle. Specifically: SPL_FI[31:8] is the value at the sampling point before the positive zero-crossing, SPL_FU[31:8] is the value at the sampling point after the positive zero-crossing, and {SPL_FU[7:0], SPL_FI[7:0]} represents the number of sampling points from the cycle before the zero-crossing. =10: When the zero-crossing count special command (0xea 0x7C) is active, it records the two sampling values before and after the first zero-crossing point following the command, with the same definition as 01. =11: Keep
7DH	SPL_FI	R	4	00	

2.1 5.4 Interrupt Register

Interrupt Configuration and Allow Register IE (0x40)

This register supports both SPI and UART. When the interrupt enable bit is set to 1 and an interrupt occurs, the IRQ_N pin outputs a low level. The write-protected register requires write enable to be enabled before configuration.

Interrupt Enable Register (IE) Address：0x40H Default value: 0x00H Read/Write		
bit	**Position Name**	**functional description**
7	SPLIE	SPLIE=0; disable waveform data update interrupt; SPLIE=1: Enables waveform data update interrupts, with the update speed set to F osc/2/128
6	FZIE	FZIE=0: Disable power freeze interrupt; =1: Enable power freeze interrupt
5	ZXIE	ZXIE=0: Disable zero-crossing interrupt; ZXIE=1: Enable zero-crossing interrupt.
4	QEOIE	QEOIE=0: disables the custom power register overflow interrupt. QEOIE=1: Enables the custom power register overflow interrupt.
3	PEOIE	PEOIE=0: Disable active power register overflow interrupt; PEOIE=1: Enables active power register overflow interrupt.
2	QFIE	QFIE=0: QF interrupt disabled; QFIE=1: QF interrupt enabled.
1	PFIE	PFIE=0: Disable PF interrupt; PFIE=1: Enable PF interrupt.
0	DUPDIE	DUPDIE=0: Disable data update interrupts; DUPDIE=1: Enable data update interrupts. The data refresh rates for PowerPA/PowerPB, IARMS/IBRMS, and URMS registers are 3.414Hz or 13.655Hz. When these data are updated, the IRQ_N pin outputs a low level.

Interrupt Flag (IF) (0x41)

Interrupt Flag Register (IF) Address：0x41H read-only		
bit	**Position Name**	**functional description**
7	SPLIF	SPLIF=0: No waveform update event occurred; =1: A waveform update interrupt occurred.
6	FZIF	FZIF=0: No power freeze event occurred; =1: A power freeze event occurred
5	ZXIF	ZXIF =0: No zero-crossing events occurred; ZXIF =1: Zero-crossing events occurred.
4	QEOIF	QEOIF=0: No overflow event occurred in the custom energy register. QEOIF=1: Custom power register overflow event occurs.
3	PEOIF	PEOIF=0: No active power register overflow event occurred. PEOIF=1: A register overflow event for active power energy has occurred.
2	QFIF	QFIF =0: No QF pulse output event occurred. QFIF =1: QF pulse output event occurs.
1	PFIF	PFIF =0: No PF pulse output event occurred. PFIF =1: A PF pulse output event has occurred.
0	DUPDIF	DUPDIF=0: No data update event occurred; DUPDIF=1: A data update event has occurred.

The IF applies to SPI and UART interfaces. When an interrupt event occurs, the hardware sets the corresponding interrupt flag to 1.

The IF interrupt flag is not controlled by the interrupt enable register IE, but by whether the

interrupt event occurs.

If the IF is a read-only register, it will be cleared after reading.

Reset Interrupt Flag (RIF) (0x42)

Reset Interrupt Flag Register (RIF)			Address：0x42H					
	Bit7	6	5	4	3	2	1	Bit0
Read:	SPLIF	FZIF	RZXIF	RQEOIF	RPEOIF	RQFIF	RPFIF	RDUPDIF

The register function is equivalent to IF.

Wave buffer status register WAVE_IF (0x46)

Wave Interrupt Flag (WAVE_IF) Address：0x46H read and write		
bit	**Position Name**	**functional description**
7	Reserved	Read-only, read as 0.
6	USAGIF	U-channel drop event flag =0: No U channel drop event occurred; =1: U channel drop event occurred. Reset after reading
5	UpeakIF	U-channel overload event flag =0: No U channel overload event occurred; =1: U channel overload event occurred. Reset after reading
4	IApeakIF	IA channel overload event flag =0: No IA channel overload event occurred; =1: IA channel overload event occurred. Reset after reading
3	IBpeakIF	IB channel overload event flag =0: No IB channel overload event occurred; =1: IB channel overload event occurred. Reset after reading
2	WAVE_ERR_IF	Data coverage error flag =0: No data overwrite error occurred; =1: Data overwrite error occurred. Clear after reading
1	WAVE_HF_IF	Wave half-full symbol The SPI read half-waveform command clears this flag. =0: The half-full waveform indicator is not active; =1: The half-full waveform indicator is triggered. Clear after reading.
0	WAVE_BUSY	Waveform buffer busy flag: =1: indicates the waveform buffer is busy; =0: Mark waveform buffer idle

Waveform Buffer Interrupt Enable Register WAVE_IE (0x47)

Wave Interrupt Enable (WAVE_IE) Address：0x47H read and write		
bit	**Position Name**	**functional description**
7	IBTH_Flag_IE	0: Disable IBTH_flag interrupt

		Enable the IBTH_flag interrupt The power supply reset to 0
6	USAGIE	=0: Disable U-channel drop interruption; =1: Enable U channel drop interrupt.
5	UpeakIE	=0: Disable U channel overload interrupt; =1: Enable U channel overload interrupt.
4	IApeakIE	=0: Disable IA channel overload interrupt; =1: Enable IA channel overload interrupt.
3	IBpeakIE	=0: Disable IB channel overload interrupt; =1: Enable IB channel overload interrupt.
2	WAVE_ERR_IF	Enable data coverage error interrupt
1	WAVE_HF_IF	waveform half full interrupt enable
0	Reserved	Read-only, output 0

2.1 5.5 System Status Registers

System status register SysStatus (0x43)

System Status Register (SysStatus) **Address：0x43H read-only**		
bit	**Position Name**	**functional description**
7	U_dc_en	The U channel is undergoing automatic DC offset correction. When the special command is enabled, the offset at position 1 will be automatically reset after correction.
6	Ib_dc_en	The IB channel is undergoing automatic DC offset correction. When the special command is enabled, the offset at position 1 will be automatically cleared after correction.
5	Ia_dc_en	The I/A channel is performing automatic DC offset correction. When the special command is enabled, the offset at position 1 will be automatically reset after correction.
4	WREN	Write enable flag: =1 Allows writing to write-protected registers; =0 Writing to write-protected registers is not allowed
3	Reserved	Read-only, read as 0.
2	IS	The MKE101R serial communication type selection pin determines the chips communication interface type. IS=0 indicates UART as the communication interface, while IS=1 indicates SPI as the communication interface.
1	SOFTRST	Reset the command flag. When the command reset is complete, this position is set to 1. It is cleared after reading. This flag can be used for resetting and recalibrating data requests.
0	RST	Hardware reset flag. Set to 1 when the external RST_N pin or power-up reset is completed. Clears after reading. Used for post-reset calibration data requests.

SPI/UART read check register RData (0x44)

The RData (0x44H) register stores the data read from SPI/UART in the previous session, which can be used for data verification during SPI/UART read operations.

SPI/UART writes the WData (0x45) register

The WData (0x45H) register stores the previous SPI/UART write data and can be used for data validation during SPI/UART operations.

2.1 5.6 Extended Registers

While retaining the original read/write register scheme, a new set of registers with 7-bit address width is introduced. Each register has a variable length, with a maximum of 32 bits. When receiving a new special command, the read/write signals and register addresses are transmitted to the new register module to enable access to the extended registers.

command name	CMD	CMD	DATA	description
extended register write	0xDF	{0, addr}	Write data	Write to the extended register
extended register read	0x5F	{0, addr}	Read data	Read from the extended register

IIC configuration register IIC_CFG (0x0)

bit	name	description	Read/Write	Reset value
15	BCHG	In the special mode, the received data is stored by swapping byte positions in pairs. 0： The received byte0 is stored in IIC_TRDAT0[7:0] The received byte1 is stored in IIC_TRDAT0s 15th to 8th bits. The byte2 received is stored in IIC_TRDAT1[7:0] The received byte3 is stored in IIC_TRDAT1[15:8]. and so on IIC_TRDAT0={byte1, byte0}; IIC_TRDAT1={byte3, byte2}; IIC_TRDAT2={byte5, byte4}; IIC_TRDAT3={byte7, byte6}; IIC_TRDAT4={byte9, byte8}; IIC_TRDAT5={byte11, byte10}; 1： The byte0 received is stored in IIC_TRDAT0[15:8]	R/W	0

		The received byte1 is stored in IIC_TRDAT0s bit 7 to 0. The byte2 received is stored in IIC_TRDAT1[15:8] The received byte3 is stored in IIC_TRDAT1s 7:0 bits. and so on IIC_TRDAT0={byte0, byte1}; IIC_TRDAT1={byte2, byte3}; IIC_TRDAT2={byte4, byte5}; IIC_TRDAT3={byte6, byte7}; IIC_TRDAT4={byte8, byte9}; IIC_TRDAT5={byte10, byte11};		
14:12	ATTM	Automatic temperature measurement interval (IIC automatically initiates read commands at intervals measured in waveform buffer fullness, i.e., two HSTX frames are sent (the chip sends one HSTX frame at half-full capacity). For example: 25x frequency division, half-full interval is 2.96ms. The measurement interval is 2.96ms*2*25=148ms.) 00:25 frequency division 001:50 Hz 010:100 Hz 011:200 Hz 100:250 frequency division 101:300 Hz 110:400 Hz 111:500 Hz	R/W	0x0
11:9	BYTNUM	Select the number of bytes for single-mode multi-byte read: 000： 2 001： 4 010： 6 011： 8 100： 10 101： 12 Other: Retain	R/W	0x0
8:7	CMDM	Select the mode for single-time sequence transmission in special mode. 00: Select 8-bit write timing 01: Select 16-bit write timing 10: Select 8-bit read timing 11: Select multi-byte read timing (number of bytes determined by BTNUM)	R/W	0
6	AUTO	Special mode automatically selects the cycle mode. When set to 1, the ONCE_KICK write cannot trigger the IIC to initiate specific timing on the bus. Only the HSTX	R/W	0

		interface can automatically trigger the IIC to initiate specific timing without MCU intervention. =0, single-use dedicated mode; =1, Auto cycle mode.		
5:2	CLKDIV	IIC clock frequency selection bit: 0000： Fosc/2/8 0001： Fosc/2/ 1 0 0010: Fosc/2/ 1 2 0011： Fosc/2/ 1 4 0100： Fosc/2/ 1 6 0101： Fosc/2/ 1 8 0110： Fosc/2/ 2 0 0111： Fosc/2/36 1000： Fosc/2/ 7 2 1001： Fosc/2/ 1 44 Other: Fosc/2/1 8	R/W	0x5
1	SP_MODE	IIC dedicated mode selection 0: General Mode 1: Dedicated Mode	R/W	0
0	IIC_EN	IIC module enable bit 1: IIC open 0: IIC is off	R/W	0

IIC control register IICCtl (0x1)

bit	name	description	Read/Write	Reset value
15:10	---	continue to have	R	0
9	SDA_PHEN	SDA IO internal pull-up 0: Enable pull-up 1: Pull-up disabled	R/W	0
8	SCL_PHEN	SCL IO internal pull-up 0: Enable pull-up 1: Pull-up disabled	R/W	0
7:4	--	continue to have	R/W	0
3	ACK	ACK signal receive and send bits When receiving data: 1: Generate an ACK signal upon receiving the ninth SCL. 0: No ACK signal is generated upon receiving the ninth SCL.	R/W	0
2:1	BUSCON	The bus control generates bits. The start command is valid when the bus is idle or the host is in the send state. The stop command is valid when the host is in	R/W	0

		the send state. When the start or stop sequence is detected, the command bit is cleared. 00: No action 01: Generate the START sequence 10: Generate the STOP sequence 11: Retain		
0	ONCE_KICK	Single startup in exclusive mode Software writes 1, and the IIC initiates sending one sequence (any of the four sequences: 8-bit write, 16-bit write, 8-bit read, 16-bit read). Software reset 0 is invalid. The hardware resets automatically. Writing this bit is invalid when AUTO is 1.	WO	0

IIC status register IIC_STA (0x2)

bit	name	description	Read/Write	Reset value
15:6	---	continue to have	R	0
5	SP_ACK_ERR	In dedicated mode, the slave ACK flag is abnormal. The software writes 1 and resets it to zero. 0: Normal; 1: Abnormal; After setting to 1, the hardware will not reset automatically; software reset is required.	R/W	0
4	BUSY	IIC bus busy flag 0: Idle; 1: Busy;	R	0
3	DIR	read/write direction flag 1: Read. 0: Write.	R	0
2	MATCH	Match the address bit and clear it when the start or stop sequence is detected. 0: Address does not match 1: Address match	R	0
1	RX_ACK	ACK flag received Write 1 to clear this position 1: No ACK received 0: ACK received	R/W	0
0	TRANC	transfer completed flag Writing 1 to this position will clear it. If the send buffer is empty when sending data or the receive buffer is full when receiving data, the transfer	R/W	0

		completion interrupt is triggered. 0: Transfer not completed 1: Transfer completed It can also function as a completion flag for dedicated mode transmission, where the bit is set to 1 after a single data transmission in dedicated mode.		

The IIC devices address register IIC_SADDR (0x3)

bit	name	description	Read/Write	Reset value
15：8	SM_ADDR	SM_ADDR[7:1]: Device address bit. Addresses cannot be written to this register during transmission. It represents the address of the slave device. SM_ADDR[0]: Host read/write direction control bit 0: Write 1: Read (Note: When using the dedicated mode, SM_ADDR[0] must be fixed to 0)	R/W	0
7:0	SR_ADDR	Slave register address. The address cannot be written to this register during transmission.	R/W	0

Note: When using general mode, only SM_ADDR can be operated.

IIC data transmission/reception register IIC_TRDATx (0x4~0x9)

IIC data register (6 sets, x ranges from 0 to 5)

bit	name	description	Read/Write	Reset value
15:8	BYTE1	Receive or send data byte 1. (8-bit write/read timing, this register is not used)	R/W	0
7:0	BYTE0	Receive or send data byte 0.	R/W	0

Note: When using general mode, you can only operate on byte0.

Waveform output control register WAVECtl (0x20)

bit	Position Name	functional description	Read/ Write	Windows default
7	Reserved	continue to have	-	-
6:5	Div_sel	buffer interval configuration =00: Cache all points; =01:2x interval buffer	R/W	0

		=10:4x interval buffer =11: Keep		
4:3	wave_sel	Data source selection: =00: Measure full-wave data =01: Measurement fundamental wave data =10: Synchronize data =11: Keep	R/W	0
2	INV_BYTE	data transmission sequence configuration =0: High byte first for waveform data =1: Low byte first for waveform data Note: This applies only to SPI/UART output mode	R/W	0
1:0	WAVE_WIDTH	channel data transmission length configuration =00: A 16-bit data sample is taken from a sampling point (wave_data[19:4]) =01:16-bit data from a sampling point (wave_data[17:2]) =1X: A sampling point captures 24-bit data (with the lower four bits padded with 0s, data format: {wave_data, 4h0}) Note: This applies only to SPI/UART output mode	R/W	0

pay attention to ：

wave_data is WAVECtl.The wave_sel selects waveform data, with 20 bits of valid data. The wave_data[19:18] register contains two symbol bits, normalized as wave_data[19:0] ÷ 2^18. The RMS value register, 24 bits of valid data, has the most significant bit fixed to 0, normalized as Rms ÷ 2^23.

The calculated valid value from wave_data[19:0] must be multiplied by 2^5 (the difference between 23 and 18 equals 5 bits) to match the metering valid value register.

WAVE_CTL.WAVE_WIDTH controls the number of valid bits in the SPI/UART output waveform data.

WAVE_CTL.WAVE_WIDTH=00: A sampling point captures 16-bit data (wave_data[19:4]). The output waveform data is processed to calculate the RMS value, which requires multiplication by 2^9 (5+4=9 bits) to match the metering RMS value register.

WAVE_CTL.WAVE_WIDTH=01: A sampling point captures 16-bit data (wave data[17:2]). The output waveform data is processed to calculate the RMS value, which requires mul

tiplication by 2^7 (5+2=7 bits) to match the metering RMS value register.

WAVE_CTL.WAVE_WIDTH=1X: A 24-bit sampling point is transmitted (with the lower four bits padded with zeros, data format: {wave_data, 4h0}). The output waveform data is processed to calculate the RMS value, which must be multiplied by 2 (5-4=1 bit) to matc h the metering RMS value register.

HSTX control register HSTXCtl (0x21)

bit	Position Name	functional description	Read/ Write	Windows default
23:20	continue to have		R	0
19	IRQ_OE	Disable data output interrupt =0: Do not output interrupt data =1: Output interrupt data	R/W	1
18	Word_chksum	Waveform data checksum calculation method configuration =0: Accumulate and settle by byte =1: Sum by word	R/W	0
17:16	BANK_NUM1	Configure the number of banks to send at full capacity =00: Do not send =01: Send 1 bank =10: Send 2 banks =11: Send 3 banks	R/W	0
15:14	BANK_NUM0	Configure the number of banks to send when half full =00: Do not send =01: Send 1 bank =10: Send 2 banks =11: Send 3 banks	R/W	0
13:8	OUT_WAIT_CNT	HSTX output enable wait configuration: The wait time is (OUT_WAIT_CNT+1) ms	R/W	0
7	PULSE_WAIT	Pulse data transmission wait time configuration =0: Send after a 12.292us pulse generation (one-byte transmission time) =1: Send after a 49.168us pulse generation (4-byte transmission time)	R/W	0
6:5	IB_WIDTH	IB channel length configuration (see	R/W	0

		WAVECtl for the relationship with valid values).WAVE_WIDTH） =00:16bit（IB[19:4]） =01:16bit（IB[17:2]） =1X:24bit（{ IB , IBcnt[1:0], 1,1}）		
4:3	IA_WIDTH	IA channel length configuration (see WAVECtl for the relationship with valid values).WAVE_WIDTH） =00:16bit（IA[19:4]） =01:16bit（IA[17:2]） =1X:24bit（{ IA , Iacnt[1:0],1,0}）	R/W	0
2:1	U_WIDTH	U-channel length configuration (see WAVECtl for the relationship with valid values).WAVE_WIDTH） =00:16bit（U[19:4]） =01:16bit（U[17:2]） =1X:24bit（{ U , Ucnt[1:0],0,1}）	R/W	0
0	INV_BYTE	data transmission sequence configuration =0: Low byte first; =1: High byte first	R/W	0

HSTX Bank enables the register HSTX_REG_OE (0x22)

bit	Position Name	functional description	Read/ Write	Windows default
15:12	BANK8_num	Number of messages sent by BANK8	WR	0
11: 10	BANK10_EN	BANK10 output enable signal: =00: No output =01: Output only when the waveform buffer is half full =10: Output only when the waveform buffer is full =11: Output when half full or full	WR	0
9:8	BANK9_EN	BANK9 output enable signal: =00: No output =01: Output only when the waveform buffer is half full =10: Output only when the waveform buffer is full =11: outputs when half full or full	WR	0
7	BANK 11_EN	BANK 11 output enable signal	WR	0
6	BANK7_EN	BANK7 output enable signal	R/W	0
5	BANK6_EN	BANK6 output enable signal	R/W	0

4	BANK5_EN	BANK5 output enable signal	R/W	0
3	BANK4_EN	BANK4 output enable signal	R/W	0
2	BANK3_EN	BANK3 output enable signal	R/W	0
1	BANK2_EN	BANK2 output enable signal	R/W	0
0	BANK1_EN	BANK1 output enable signal	R/W	0

- When operating, users must configure BANK9_EN and BANK10_EN according to the waveform buffer mode (single-channel or dual-channel) to achieve the half-wave time transmission requirement for bank9 and bank10 registers.
- This register cannot be modified after HSTX_EN is enabled.

HSTX enable register HSTX_EN (0x23)

bit	Position Name	functional description	Read/ Write	Windows default
7:1	continue to have		R	0
0	HSTX_EN	HSTX enable signal	WR	0

HSTX reference value register

bit	Position Name	functional description	Read/ Write	Windows default
31:0	HSTX_PFDAT	The pulse data value output when a PF pulse occurs	WR	0x800A20AA

- This register cannot be modified after HSTX_EN is enabled.

HSTX QF reference value register

bit	Position Name	functional description	Read/ Write	Windows default
31:0	HSTX_QFDAT	The pulse data value output when a QF pulse is received	WR	0x800C40CC

- This register cannot be modified after HSTX_EN is enabled.

HSTX FPFDAT (0x26) reference value register

bit	Position Name	functional description	Read/ Write	Windows default
31:0	HSTX_FPFDAT	The pulse data value output when the FFPulse arrives	WR	0x800E60EE

- This register cannot be modified after HSTX_EN is enabled.

HSTX IRQDAT reference value register (0x27)

bit	Position Name	functional description	Read/ Write	Windows default
31:0	HSTX_IRQDAT	The pulse data value output during an interrupt	WR	0x800820A8

●This register cannot be modified after HSTX_EN is enabled.

The HSTX pin function enables the register HSTX_TXOUT (0x2B)

bit	Position Name	functional description	Read/ Write	Windows default
7:1	continue to have		R	0
0	HSTX_TX_OUT_SEL	TX pin multiplexing HSTX function enable signal 0: The TX pin operates normally for UART transmission. 1: The TX pin supports HSTX functionality. When the HSTX module is enabled, this feature becomes available.	WR	0

HSTX IOCFG register (0x2C) for pulse selection

Address: 0x2C; word length: 4 bytes; default: 0x610

bit	Position Name	functional description	Read/ Write	Windows default
31:12	continue to have		R	0
11:8	FPF_SEL	Selection of FPF Input Signal Source for HSTX =4h0: FPF outputs CF1 (PF) =4h1: FPF outputs CF2 (QF) =4'h2：FPF output CF3 =4'h3：FPF output CF4 =4'h4：FPF output CF5 =4'h5：FPF output CF6 =4h6: FPF outputs CF7 (default: FPF) =4'h7：FPF output CF8 =4'h8：FPF output CF9 =4h9: FPF outputs IRQ (interrupt request)	RW	6

		=4hA: FPF output ZX (zero-crossing output) =Others: Keep =4hF: FPF does not output		
7:4	QF_SEL	Selection of QF Input Signal Source for HSTX =4h0: QF outputs CF1 (PF) =4h1: QF outputs CF2 (default: QF) =4'h2：QF output CF3 =4'h3：QF output CF4 =4'h4：QF output CF5 =4'h5：QF output CF6 =4'h6：QF output CF7 =4'h7：QF output CF8 =4'h8：QF output CF9 =4h9: QF outputs IRQ (interrupt request) =4hA: QF output ZX (zero-crossing output) =Others: Keep =4hF: QF does not output	RW	1
3:0	PF_SEL	Selection of PF Input Signal Source for HSTX =4h0: PF outputs CF1 (default: PF) =4h1: PF outputs CF2 (QF) =4'h2：PF output CF3 =4'h3：PF output CF4 =4'h4：PF output CF5 =4'h5：PF output CF6 =4'h6：PF output CF7 =4'h7：PF output CF8 =4'h8：PF output CF9 =4h9: PF outputs IRQ (interrupt request) =4hA: PF output ZX (zero-crossing output) =Others: Keep =4hF: PF does not output	RW	0

Leakage current protection configuration register IBDET_CFG (0x30)

bit	Position Name	functional description	read-write	Reset value
7:4	---	continue to have	R	0
3	IB_Trigo_en	IB_Trig Output Multiplexing: IRQ Control 0: IB_Trig is not multiplexed to IRQ (default control mode in PINCFG). 1: IB_Trig is multiplexed to IRQ. Description: 1) Fast Response Mode: Default value is 1 upon power-up, with IB_Trig multiplexed to IRQ. The MCU can modify the control mode. 2) Normal Mode: Default value is 0 upon power-up, with IB_Trig not multiplexed to IRQ. Note: When the MOD pin is 1, the default reset of IRQ upon power-up is IB_Trig.	R/W	0
2	IB_Trig_SW	MCU Trig signal state register: 0 = inactive, 1 = active. The MCU performs write, set, and reset operations without clearing.	R/W	0
1	IB_Trig_hw_off	The hardware half-wave threshold detection of the IB channel is triggered by the IB_Trig signal. The shielding control is enabled (0) or disabled (1), with the fast-response mode automatically switching to 0 upon power-on.	R/W	1
0	IBTH_Det_en	The IB channel threshold detection enables control: 0 = disabled, 1 = enabled. When hardware threshold detection is active, the signal is automatically reset to 0. The MCU enables or disables it through write operations.	R/W	1

Leakage current detection flag register IBDET_FLG (0x31)

bit	Position Name	functional description	read-write	Reset value
7:3	continue to have	continue to have	R	0
2	IB_Trig	IB Trig outputs a status signal (not a register signal) in fast response mode to the IRQ pin	R	0
1	IB_Trig_HW	The hardware detection of IB triggers the Trig signal. State register 0: Invalid level. 1: Valid level. Hardware valid detection triggers the set bit; MCU writes 1 and clears 0 (no read clearing).	R/W	0
0	IBTH_Flag	IB Hardware Detection Status Register 0: Indicates the half-wave effective value of the IB channel has not exceeded the threshold. 1: Indicates the half-wave effective value of the IB channel has exceeded the threshold. Hardware valid detection triggers the bit is set to 1, MCU writes 1 and clears 0.	R/W	0

Set the zero-crossing threshold register ZXOTU (0x32)

address	name	read-write	byte	Windows default	function declaration
32H	ZXOTU	R/W	2	0000h	The zero-crossing threshold register is configured to generate a zero-crossing signal only when the high 16 bits of the valid value exceed this threshold, ensuring the voltage line frequency is accurately measured. The default value is 0, which represents the value 16h100

Event detection threshold register USAG/xPEAK (0x33~0x36)

offset address	33H	34H	35H	36H
register	USAG	UPEAK	IAPEAK	IBPEAK
Windows default	0	0	0	0

The event threshold register includes: voltage drop threshold register USAG, current channel A peak detection threshold register, current channel B peak detection threshold register, voltage channel peak detection threshold register.

The voltage drop threshold register is a 16-bit unsigned number. This function remains disabled when the value is zero. Upon writing a non-zero value, the drop detection is activated. The threshold is compared with the high 16 bits of the 24-bit waveform samples from the ADC sampling channel, with the number of detected half-cycles determined by SYSCON2.usag_cfg[7:0].Sag_Freq_sel=0, sag refers to a 50Hz application, with a fixed half-cycle duration of 10ms; EMUCON.Sag_Freq_sel=1, sag refers to a 60Hz application cycle, with a fixed half-cycle duration of 8.333ms. When the drop duration exceeds usag_cfg, a trigger voltage drop event is activated, and the detection result includes an interrupt report.

The peak detection threshold register is a 16-bit unsigned number. This function remains disabled when the value is zero. Upon writing a non-zero value, the system initiates drop detection by comparing the threshold with the upper 16 bits of the 24-bit waveform samples from the synchronous sampling channel. If the waveform sample value exceeds the threshold, an overload event is triggered, and the detection result is reported via an interrupt.

Reactive power gain registers GQA/GQB (0x37~0x38)

Power Gain Register A(GQA)			**Address: 0x37h Default Value : 0000H**				
	Bit15	**14**	**13**	**12 … 3**	**2**	**1**	**Bit0**
Read: / **Write:**	GQA_15	GQA_14	GQA_13	GQA_12…GQA_3	GQA_2	GQA_1	GQA_0
Reset:	0	0	0	0	0	0	0
Power Gain Register A(GQB)			**Address: 0x38h Default Value : 0000H**				
	Bit15	**14**	**13**	**12 … 3**	**2**	**1**	**Bit0**
Read: / **Write:**	GQB_15	GQB_14	GQB_13	GQB_12…GQB_3	GQB_2	GQB_1	GQB_0
Reset:	0	0	0	0	0	0	0

It includes two registers: GQA and GQB, which are in binary complement format with the most significant bit as the sign bit.

GQA corrects reactive power in current channel A and voltage channel. GQB corrects gain in current channel B and voltage channel.

The correction formula is: Q1=Q0 (1 + GQS)

GQS is the normalized value of gain correction register. See the calibration method in chapter 3 for the usage.

Note: If the GQA/GQB register (extended 0x37/0x38) is set to the default value 0, the reactive power correction uses the gain correction register GPQA/GPQB (0x5/0x6). If the GQA/GQB register (extended 0x37/0x38) is set to a non-zero value, the reactive power correction uses the

GQA/GQB register (extended 0x37/0x38).

When the external crystal oscillator operates at 5.5296 MHz, the GQA/GQB is recommended for reactive power gain correction. The correction value is calculated as GQ x = GPQ x + 0x11, where GPQx represents the correction value for active power 1.0.

2.1 5.7 Special Orders

command name	command register	data	description
Write enable command	0xEA	0xE5	Enable write operation
write protection command	0xEA	0xDC	Disable write operations
Channel A select command	0xEA	0x5A	The command to set current channel A designates channel A as the current channel for calculating active and reactive power. The system accepts the command only after the write enable is set, and the CHNSEL bit in the metering status register reflects the execution result of the command.
Channel B select command	0xEA	0xA5	The command to set current channel B designates channel B as the current channel for calculating active and reactive power. The system accepts the command only after the write enable is set, and the CHNSEL bit in the metering status register reflects the execution result of the command.
command reset	0xEA	0xFA	The reset command functions as an external PIN reset. The system only accepts this command after enabling the write function. We recommend that the customers CPU perform a command reset or PIN reset prior to meter initialization.
TX pin zero-crossing output enable	0xEA	0x6C	In UART communication mode, setting this command activates the TX pin to output an IA zero-crossing signal, typically a 10ms square wave. The TXCFG bit in the metering status register indicates the commands execution status: TXCFG=1 enables zero-crossing output, while TXCFG=0 disables it.
TX pin zero-crossing output disabled	0xEA	0xC4	Disable the zero output function and restore the TX function of the UART communication port. The special command register can also be reset to the disabled state by pulling low the UART RX pin for

			12ms.
start zero counting	0xEA	0x7C	The measurement chip uses the command receipt time as a time reference, calculates the time difference between voltage zero-crossing and this reference, and stores the result in the ZXCNT (0x34H) register.
trigger waveform buffer	0xEA	0x87	Enable or disable waveform buffering
Configure the read waveform pointer	0xEA	0xA7	Configure the address of the read waveform pointer
single read waveform	0xEA	0xA3	Read a single waveform data, including 16-bit waveform data. After reading, the pointer increments automatically.
continuous read waveform	0xEA	0xAE	Read the waveform data in continuous mode, extracting the waveform between the start and end addresses in one go. After reading, the pointer stops at (END_ADDR+1).
Read half of the SRAM waveform	0xEA	0xAC	After the startup command, read the half-waveform of SRAM.
Automatic DC offset correction for I/A channels	0xEA	0xEA	The DC bias auto-correction function of IA channel is started, the correction points are the sampling points of 16384 synchronous sampling channels, the 16384 sampling points are directly accumulated and averaged, the result is stored in 20bit DC offset correction register DCIA.
IB channel DC offset auto-correct	0xEA	0xEB	The DC bias auto-correction function of IB channel is started, and the correction points are the sampling points of 16384 synchronous sampling channels. The 16384 sampling points are directly accumulated and averaged, and the result is stored in 20bit DC offset correction register DCIA.
U-channel DC offset auto-correct	0xEA	0xEC	The DC bias auto-correction function of U channel is started, and the correction points are the sampling points of 16384 synchronous sampling channels. The 16384 sampling points are directly accumulated and averaged, and the result is stored in 20bit DC offset correction register DCIA.
UART baud rate switching	0xEA	0xB3	0x24 sets the UART baud rate to Fosc/2/ (15×47+41) 0x48 sets the UART baud rate to Fosc/2/ (15×24+13) 0x96 sets the UART baud rate to Fosc/2/ (15×12+6) 0x19 sets the UART baud rate to Fosc/2/(15×6+3) The baud rate of the 0-AA UART is determined by

			the hardware. Other values: The baudrate remains unchanged
Enable PAD transparent transmission	0xEA	0x66	0x24 receives input from RX pin and outputs from IRQ pin 0x48: Input from RX pin, output from PF 0x96 Input from RX pin to QF output Other values are invalid

Write protection scope:

The 0x00H-0x1AH register stores calibration parameters, 0x20h-0x21h contains fast pulse registers, and 0x40h is the interrupt enable register. These registers can only be modified after enabling them with specific commands, as detailed in the table above.

Note: All special commands, including waveform buffer read/write commands, fall within the reliability range of Wdata.

3 Calibration Method

3.1 Overview

MKE101R provides a comprehensive calibration solution for software-based instrument calibration, achieving both active and reactive power accuracy at the 0.5S class level. The calibration methods of MKE101R include:

- The meter constant (HFConst) is adjustable.
- Provide gain and consistency correction for A/B channels
- Provide phase correction for A/B channels
- Provide active, reactive, and RMS offset correction for A/B channels
- provide reactive power phase compensation
- Provide small signal acceleration correction
- Enable automatic meter calibration

3.2 Calibration Process and Parameter Calculation

The standard energy meter can be used for calibration. The active power and custom energy pulses (PF/QF) can be directly connected to the standard meter via optocouplers, and the MKE101R can then be calibrated based on the error readings from the standard energy meter.

3.2.1 Calibration Process

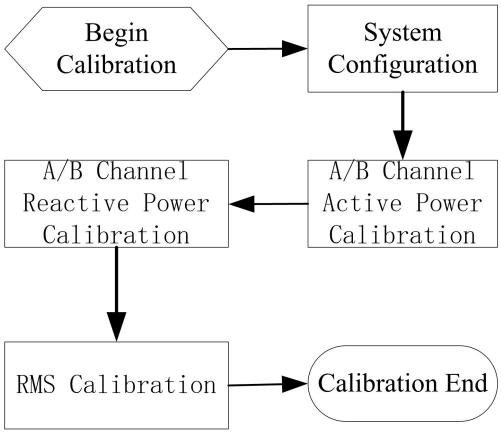


Figure 3-1 Calibration Process

3.2.2 Parameter Settings

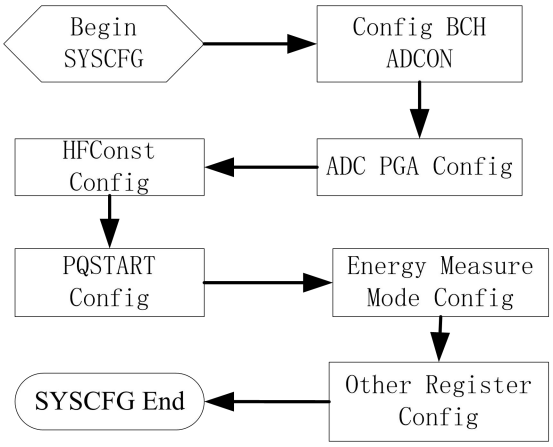


Figure 3-2 Parameter Setting Flow

HFConst parameter calculation:

The calculation formula for HFConst is as follows:

HFConst＝INT[16.1079*Vu*Vi*10^11/(EC*Un*Ib)]　@Fosc3.579545MHz

HFConst＝INT[24.883 2*Vu*Vi*10^11/(EC*Un*Ib)]　@F osc 5.5296MHz

Vu: The voltage in the voltage channel at rated input voltage (pin voltage × PGA)

Vi: Voltage across the current path (pin voltage × PGA) at rated current input

Un: Rated input voltage; Ib: Rated input current; EC: Meter constant

3.2.3 Active Power Correction

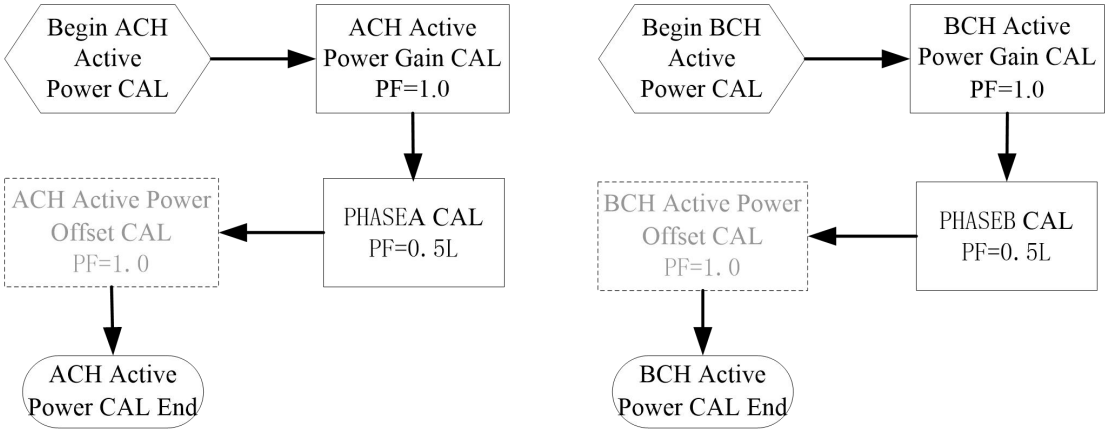


Figure 3-3 Active Power Correction Process

1. The power gain correction for channel A can be configured via the GPQA register, with the following calculation method:

   If the standard table reads an error of err on channel A at 100% Ib and PF=1:

   $$Pgain = \frac{-err}{1+err}$$

   If Pgain>=0, then GPQA=INT[Pgain*2^{15}]

Otherwise, if Pgain is less than 0, then GPQA equals INT[2].^{16}+Pgain*2^{15}]

The B-channel power gain correction can be implemented by configuring the GPQB register, following the same procedure as for GPQA.

2. A/B channel phase correction register calculation method

If the standard table reads an error (err) at channel A/B with 100% Ib and PF=0.5L, the phase compensation formula is:

$$\theta = \text{Arcsin}\frac{-err}{\sqrt{3}}$$

For the relationship between 50Hz, PHSA/B, 0.02°/LSB @Fosc3.579545MHz, and 0.013°/LSB @Fosc5.5296MHz, then there is

Fosc3.579545MHz

If>=0, PHSA/B = INT(0.02°)θ θ

If <0, PHSA/B = INT(2^8+/0.02°)θ θ

F osc 5.5296MHz

If>=0, PHSA/B = INT(0.013°)θ θ

If <0, PHSA/B = INT(2^8 + 0.013°)θ θ

3. The active offset correction is an effective method to improve the active precision of small signals when the external noise (PCB noise, transformer noise, etc.) is large and the energy obtained by integration affects the small signal precision. If the external noise has little effect on the active precision of small signals, this step can be ignored.

3.2.4 Reactive Power Correction

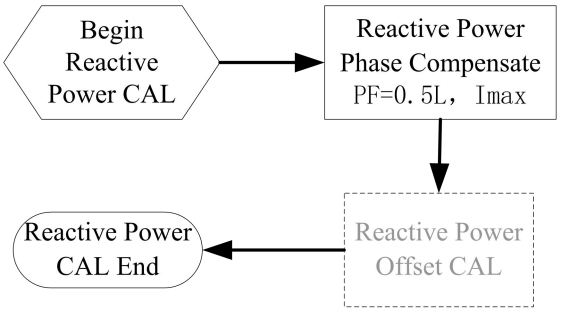


Figure 3-4 Reactive Power Correction Process

After active power correction, simply input an empirical value (see Appendix 1) into the reactive power phase correction register according to the signal frequency to ensure the reactive power error stays within 0.05%. For higher precision, apply the revised reactive power phase correction method described in Section 3 for both phase and offset corrections.

1、reactive power phase correction

The reactive power phase compensation value Qphs is calculated from the error of Ib and PF=0.5L (30^o), and then written into the reactive power phase compensation registers QPhsCal and QPhsCal 2.

The calculation method of reactive power phase compensation register is as follows:

If the standard table reads an error of err at channel A, I b, and PF=0.5L (30º), then:

α= err/ cot(θ) = err * 0.5774。

If α>=0, then Qphs=INT[α*2^{15}]; If α <0, then Qphs = INT[2^{16}+α*2^{15}]

Note: Since Qphs calculation requires active power, this step must be performed after active power correction.

2、reactive power offset correction

When the current input is zero, the value of the reactive power register is read (it can be read several times and averaged), and the last 4 bits of its 32-bit complement are written into the reactive power Offset correction register RPOSA/RPOSA.

When the external noise (PCB noise, transformer noise, etc.) is large and the energy obtained from noise integration affects the accuracy of small signal reactive power, reactive power offset correction is an effective method to improve the accuracy of small signal reactive power. If the external noise has little impact on the accuracy of small signal reactive power, this step can be ignored.

3、Revision of reactive power phase correction value

To improve reactive power error, the reactive phase correction value can be adjusted under the following two scenarios.

1) When the frequency of the measured signal changes, the reactive power phase compensation value must be recalculated using the formula QPhsCal=QPhs-13.469296 * x + 672.10022, where QPhs is the corrected reactive power phase register code value at 50Hz, and x is the frequency value (e.g., 60Hz). For example, if the reactive power phase compensation value calculated from the reactive power error is 0xFFFE at 50Hz, then at 60Hz, the value QPhsCa=0xFFFE-13.469296 * 60 + 672.10022= -138.057 = 0xFF76.

2) When the active power gain correction value exceeds 10%, the reactive power phase compensation value should be revised to QPhsCal=QPhs*(1+GPQA). The compensation formula for reactive power is Q2 = Q1-QPhs*P1, where Q2 is the compensated reactive power, Q1 is the pre-compensation reactive power, and P1 is the corrected active power. However, the chip actually uses the active power P0 before the GPQA effect. Therefore, the compensation formula for reactive power should be revised to Q2 = Q1-QPhs*(1+GPQA)*P0.

3.2.5 Valid Value Correction

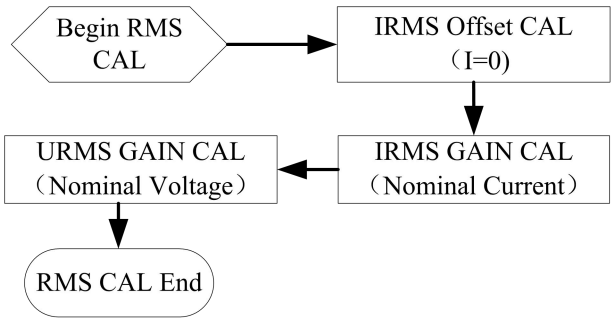


Figure 3-5 RMS Correction Process

explain ：

1. Current offset correction improves the RMS accuracy of small signal currents

IARMSOS register calculation process:

1) Set up the standard test bench to ensure U=Un and the current channel input Vi=0;

2) Wait for the DUPDIF flag to be updated;

3) The MCU retrieves the IARMS register value and temporarily stores it;

4) Repeat steps 2 and 3 eleven times. Discard the first data point. The MCU calculates the average of the last ten data points to obtain the average value.

5) Calculate the square of Iave, Iave^2;

6) Calculate the 32-bit binary complement, then use bits 23-8 to set bit 15-0 of IRMSOS to obtain IRMSOS.

7) Offset correction for valid values completed

The calculation process of IBRMS correction formula and IBRMSOS register is the same.

2. After calibrating the current offset, the MCU performs correction of the A/B channel current conversion coefficients KiA/KiB and voltage conversion coefficient Ku, with the calculation process as follows:

If the IARMS register reading is RMSIAreg at rated current Ib, then

KiA＝Ib/RMSIAreg

KiA is the ratio of the rated value to the corresponding register at the rated input.

The calculation process of B channel conversion coefficient KiB and voltage conversion coefficient Ku is the same.

3.2.4 Examples

The design involves a sample circuit with a 220V (Un) and 5A (Ib) rated input, featuring a 3200 EC (Equivalent Circuit) table constant. The crystal oscillator operates at 3.579545 MHz. Channel A employs a 350 μΩ manganized copper for current sampling, with a 16x analog gain. Channel B utilizes a current transformer for sampling, configured with a 1x analog gain. Voltage input is achieved through a resistor divider, maintaining a 1x analog gain, while the chip pin voltage is set at 0.22V.

1. Calculate HFConst

Vu＝0.22V;　Vi＝5*0.00035*16＝0.028V; EC=3200; Un=220; Ib=5.

HFConst=[16.1079*Vu*Vi*10^11/(EC*Un*Ib)]= 2818

After rounding, HFConst equals B02 H (2818). Write this value to the HFCONST register.

2. A channel active correction

1) Gain correction for channel A

The power source outputs a 220V,5A signal with a power factor of 1, and the standard meter displays an error of 1.2%.

Pgain＝-0.012/(1+0.012)=-0.01186

The value is less than 0 and must be converted to twos complement. Therefore, -0.01186*2^15+2^16=0xFE7BH

Write FE7Bh to the GPQA register to complete the gain correction for channel A.

2） A-channel phase correction

After adjusting the resistive gain, the power factor was set to 0.5L. The standard meter indicated an error of-0.4%.

θ=ArcSin（-(-0.004)/1.732）=ArcSin 0.0023 ＝ 0.1323^0

phs=INT[0.1323/0.02]=6

After rounding, the value becomes 0x06H, which can be written into the PHSA angle

correction register.

3) A-channel active offset correction

When the current input is zero, the active power register value 0xfffff50f is read (averaging can be performed after multiple readings). Its 32-bit complement is 0x00000AF1, and the last 4 bits 0x0AF1 are written into the active bias correction register.

The B channel active correction is similar to the A channel.

3. reactive power correction

1)reactive power phase compensation

After active power correction is completed, only phase compensation correction is required for reactive power. At the 0.5L (30º) point of reactive power, the standard meter displays an error of-0.04%, then

α= -0.0004*0.577= -0.0002308<0, Qphs=INT(2^16-0.0002308*2^15)=65528=0xfff8

The hexadecimal number FFF8 is written into the reactive power phase compensation register.

2) Reactive power offset

When the current input is zero, the value of the reactive power register (0xFFFFF47D) is read (averaging can be performed after multiple reads). Its 32-bit complement is 0x00000B83, and the last 4 bits (0x0B83) are written into the reactive bias correction register.

4. effective value correction

The chip provides a current RMS bias correction register. When the current input is zero, the value of the current RMS register is 0x000483 (which can be read multiple times for averaging), and the decimal value is 1155.

Calculate the square and then find its ones complement: 1155*1155=1334025=0x145B09, the 32-bit ones complement is 0 xffeba4f6.

Write the middle 4 digits 0xeba4 into the current effective value bias correction register.

The conversion factor is calculated by MCU.

4 DC Application Description

4.1 Overview

The MKE101R enables DC measurement, differing from AC measurement by requiring additional DC bias correction, as detailed below.

4.2 Basic Parameters

HFconst formula:

HFconst = INT[(16.1079*Vu*Vi*10^11) / (Un*Ib*Ec)] @F osc 3.579545MHz

Vu: The voltage channel ADC input signal (pin voltage × PGA), typically set to approximately 0.1–0.22V.

Vi: Current channel ADC input signal (pin voltage × PGA), typically set to 0.075V.

EC: Meter pulse constant (user-defined), e.g. 3200

Un: Rated voltage V,

Ib： rated current A

Clear other calibration parameters to default values.

Note: The value of HFConst, determined by user-defined EC and other parameters, should not exceed 65535.

4.3 DC OFFSET Correction

4.3.1 Register Configuration

Set SYSCON[5:4] and SYSCON[3:2] in the SYSCON register to 0x0 to configure the U and IB channel ADCs to 1x gain. Set SYSCON[1:0] to 0x3 and SYSCON2[1:0] to 0x0 to configure the IA channel ADC to 16x gain (other multipliers are available, but users should determine the appropriate value based on signal amplitude to ensure the signal remains within the ADCs 0-1V measurement range). In the EMUCON register, disable the high-pass enable for the IA/IB/U ADC channels by setting EMUCON[14] to 0x1 and EMUCON[6:5] to 0x3.

4.3.2 Calculate the average of effective values

Connect to ground, measure the RMS values of IA, IB, and U three times, then calculate the average of each RMS value.

IARMS average value

IBRMS average value

URMS average value

4.3.3 DC OFFSET Correction

Since the measured value is positive, while the DC offset may be either positive or negative, a

verification process is required after writing the DC offset: After the write operation stabilizes for 2 seconds, compare the measured value with the pre-write value. If the post-write value decreases toward 0, the correction is complete. If the post-write value increases toward twice the original value, invert the pre-write value and rewrite it. As shown below:

1. First write

The IARMS1 average values BIT[23:8] is first written into the DCIAH register (0x13), and BIT[7:4] is then written into the DCL register (0x16) of DCL[3:0].

The average value of IBRMS1 is written to the BIT[23:8] field of the DCIBH register (0x14), and the BIT[7:4] field of the DCL register (0x16) is written to the BIT[7:4] field of the DCL register.

The average value of URMS1 is written to the BIT[23:8] register of DCUH (0x15), and the BIT[7:4] is written to the BIT[11:8] register of DCL (0x16).

2. Verification

After a 2-second delay, measure the valid values of IA, IB, and U three channels 10 times, then calculate the average valid values IARMS2, IBRMS2, and URMS2. If the valid values decrease compared to the uncorrected state, the correction is complete. If the values increase to approximately twice the original, proceed to the next step.

3. Take the inverse and rewrite

The IARMS1 average value is written to BIT[23:8] of the DCIAH register, and BIT[7:4] is written to DCL[3:0] of the DCL register.

The BIT[23:8] of the IBRMS1 average value is written into the DCIBH register, while the BIT[7:4] is written into the DCL registers DCL[7:4].

The BIT[23:8] of the average value of ~URMS1 is written into the BIT[7:4] of the DCL register in the DCL register.

4.4 Effective Value OFFSET Correction

After completing the DC offset correction, during the 2-second stabilization period, measure the RMS values of IA and IB currents 10 times, then calculate their respective averages to perform RMS offset correction using the following formula:

IARMSOS=～［(IARMS multiple average) ^ 2/2 ^ 8］low 16 bits

IBRMSOS=～［(IBRMS multiple average) ^ 2/2 ^ 8］low 16 bits

Write the calibration value IARMSOS to the Offset Compensation Register IARMSOS (0x0E) in the valid value of Current Channel A.

Write the calibration offset IBRMSOS (0x0F) to the current channel Bs valid value offset compensation register.

4.5 Conversion Coefficient

The standard source reads the effective voltage value V and effective current value I from the metering chip, then calculates:

Kv=Un/V; the voltage conversion factor, which is multiplied by the register measurement to obtain the input voltage (v)

Ki=Ib/I; current conversion factor, which, when multiplied by the register measurement, yields the input current (A)

Kp 3 6 3 5795/4 0^ 2/(2^32 HFCons EC) @Fosc3 579545MHz Kp 3 6 5 5296/4 0^ 2/(2^32 HFCons EC) @Fosc5 5296MHz

Power conversion factor. Multiply this factor by the register measurement to obtain the input power (W).

4.6 Power Gain Correction

For the standard source, add Un and Ib to read the active power value (read as a multi-point average) P measured. Calculate using the correction formula: ERR= (P measured * Kp-Un*Ib) / (Un*Ib)

P test: Active power register values (0x26/0x27)

Kp: The power conversion coefficient determined in the previous step

Un: Voltage applied to the standard source

Ib: Current added to the standard source PGAIN=-ERR/(1+ERR)

If Pgain>0, the correction value is Pgain*2^15; if Pgain<0, the correction value is Pgain*2^15+2^16. The correction value is written into the power gain correction register GPQA/B (0x05/0x06).

4.7 Active Offset Correction

4.7.1 Power Method Correction

Apply 5%Ib current to the standard source, Un, then measure the power register value of the metering chip. Calculate the average value P over at least 20 measurements, compare it with the power value P0 from the standard meter, and compute the power offset (P offset).

APOSA= [P0 × (1/Kp) -P] / (1 + GPQA normalization)

P: Average measurement value of the chip

P0: Standard table display power

Kp: Power conversion coefficient

GPQA normalization: normalized power gain value

If APOSA>0, the correction value is APOSA. If APOSA<0, the correction value is APOSA+2^16.

4.7.2 Error Method Correction

Apply 5%Ib current to the standard source, Un, then measure the power register value of the metering chip. Calculate the average value P over at least 20 measurements, compare it with the error err of the standard meter, and compute the power OFFSET value.

APOSA = (P0*1/Kp)*(-err)/(1+GPQA normalization) (when err<0)

=2^16 + (P0*1/Kp)*(-err)/(1+GPQA normalization) (when err>0)

APOSA: active power offset correction value

P0: Standard table shows power

err: Standard table display error

Kp: Power conversion factor

GPQA normalization: normalized power gain value

Write the offset value into the active power offset register APOSA (0x0A).

Note 1): GPQA normalization formula:

GPQA normalization: =GPQA/2^15; the most significant bit of the GPQA register (0x05) = 0

GPQA normalization: = (GPQA-2^16) / 2^15; the most significant bit of the GPQA (0x05) register is 1

2) The offset correction for the active bias in path B is identical to that in path A.

5 Communication Interface

- Both SPI and UART interfaces support 5V/3.3V voltage.
- The MKE101R only supports UART serial communication.

5.2 UART Interface

The key features of the UART interface in MKE101R are as follows:

- The device operates in mode with half-duplex communication and a 9-bit UART (including parity bit), compliant with standard UART protocol.
- The MKE101R supports four baud rate configurations via hardware pins: 2400/4800/9600/19200bps@Fosc3.579545MHz.
- The frame structure includes a checksum byte, ensuring security and reliability.
- 5V/3.3V compatible

5.2.1 Description of UART Interface Signals

TX: Data transmission pin of the UART slave (MKE101R);
RX: Data receiving pin of the UART slave (MKE101R);

5.2.2 UART Data Byte Format

The UART is a 9-bit asynchronous communication port, where a byte of data consists of 11 bits: the StartBit (0), the data bits (with the least significant bit first), a Parity Bit (the 9th bit), and a Stop Bit (1). As shown in the figure below:

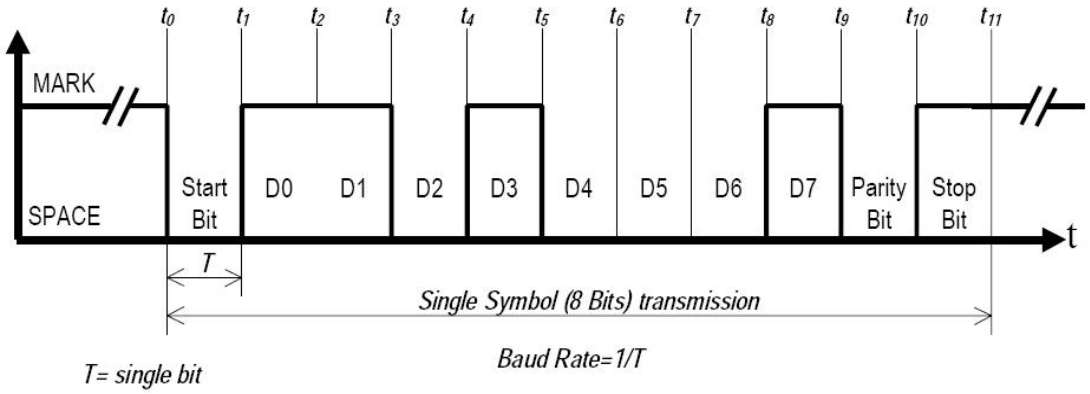


Figure 4-5 UART Data Byte Format

5.2.3 UART Frame Format

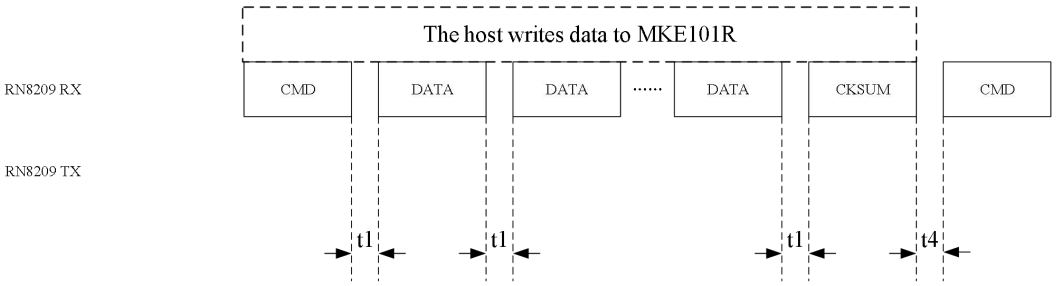
The MKE101RUART communication frame format is illustrated in the diagram and table below:

name	explain
CMD	Command byte, sent by the host CMD[7]: Indicates the command category; 0 for read operations, 1 for write operations; CMD[6:0]: The internal register address of the selected MKE101R device If CMD[7]=1 and CMD[6:0]=0x6A, this operation is a special command.
DATA	Data byte; read operations are sent from the slave end, and write operations are sent from the master end. If the register address corresponds to a multi-byte register, transmit the most significant byte first.
C H KS U M	Checksum byte; read operations are sent by the slave, write operations by the master The checksum algorithm is as follows: CheckSum[7:0] = ~(CMD[7:0] + DATAn[7:0] + …… +DATA1[7:0]) Sum the command and data, discard the carry, and invert the final result bit by bit.

command name	command byte	data byte	description
read command	{0,REG_ADR[6:0]}	RDATA	Read the data from the register at address REG_ADR[6:0] in the device. Note: Invalid address read. Return value is 00h.
Write command	{1,REG_ADR[6:0]}	WDATA	Write data to the register at address REG_ADR[6:0] in the device.
Write enable command	0xEA	0xE5	See section 2.13.6 Special Orders.
write protection command	0xEA	0xDC	
command reset	0xEA	0xFA	
trigger waveform buffer	0xEA	0x87	Refer to Section 2.12.3 on waveform buffering and read commands.
Configure the read waveform pointer	0xEA	0xA7	
single read waveform	0xEA	0xA3	
continuous read waveform	0xEA	0xAE	

5.2.4 UART Write Operation

The write operation is initiated by the host, which sends a command byte. If it is a write command, the slave continues to receive the subsequent data bytes and checksum byte sent by the host. As shown in the figure below:

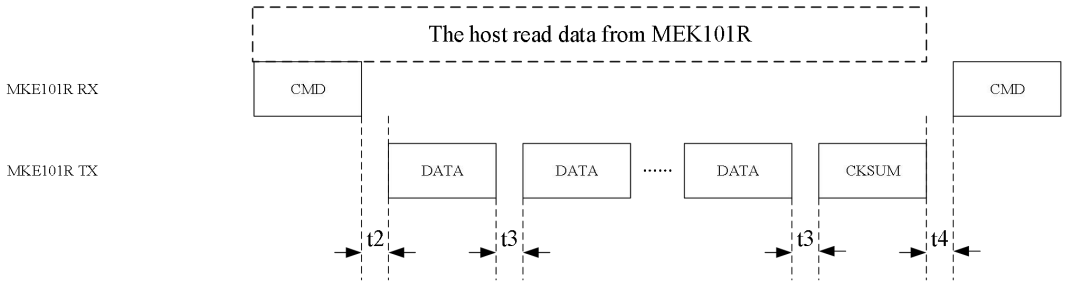


matters need attention ：

1. A 9-bit UART consists of 11 bits: the start bit (0), data bits (with the least significant bit first), a parity bit (the 9th data bit), and a stop bit (1).
2. The sending end calculates and transmits the parity bit, and the receiving end determines the validity of the byte transmission based on the parity bit; if a byte is erroneous, the subsequent byte is considered the start of a new frame.
3. Multi-byte register, first transfer the high byte content, then transfer the low byte content;
4. The time interval t1 between host data transmission bytes is controlled by the host side, with no restrictions on MKE101R, and t1 must be greater than or equal to 0ns.
5. The inter-frame interval t4 is controlled by the host side, with no restrictions on MKE101R, and t4 must be greater than or equal to 0ns.
6. The register with write protection must be written with write enable command before the write operation.
7. The host calculates and sends the checksum, and the slave determines whether the frame transmission was successful based on the checksum.

5.2.5 UART Read Operation

The read operation is initiated by the host, which first transmits the read command byte. Subsequently, the MKE101R transceiver sends the read data byte and read checksum byte. As illustrated in the figure below:



matters need attention ：

1. A 9-bit UART consists of 11 bits: the start bit (0), data bits (with the least significant bit

first), a parity bit (the 9th data bit), and a stop bit (1).

2. The sending end calculates and transmits the parity bit, while the receiving end determines the validity of the byte transmission based on the parity bit. If the byte parity check fails, the receiving end considers the current frame erroneous and terminates the process.
3. Multi-byte register, first transfer the high byte content, then transfer the low byte content;
4. The time interval t1 between host data transmission bytes is controlled by the host side, with no restrictions on MKE101R; t1 must be at least 0ns.
5. The time interval t2 between the hosts byte transmission and the slaves byte reception is controlled by the slave, where t2 equals half of the transmission time T (T being the transmission time per bit).
6. The time t3 between slave machine transmissions is controlled by the slave machine, where t3 equals T (T being the transmission time per bit).
7. The frame interval t4 is controlled by the host side, with no restrictions on MKE101R; t4 must be greater than or equal to 0ns.
8. The host calculates and sends the checksum, and the slave determines whether the frame transmission was successful based on the checksum.

5.2.6 Reliability Design of UART Interface

The reliability design of UART interface includes the following aspects:

- Configure hardware pins for baud rate, ensuring safety and reliability
- The UART data byte transfer features bit parity (even parity) functionality.
- The UART Communication Frame Transmission with Checksum Function
- The result of the configuration of the hardware pin is reflected in the register.
- register check function

  1. The verification register EMUStatus is provided to store the checksum of the internal calibration register.

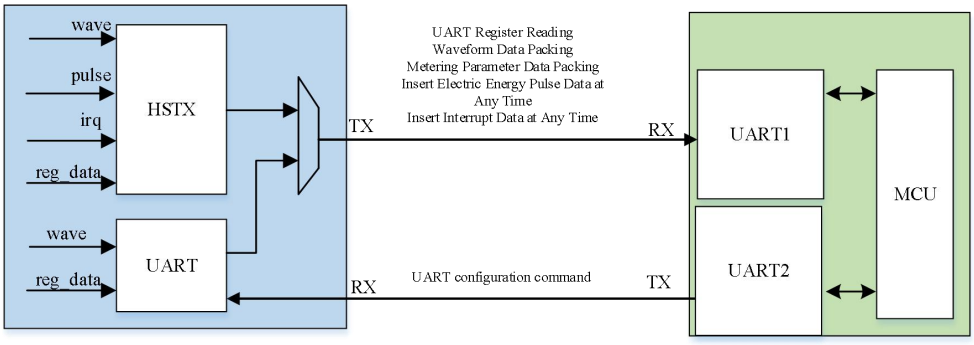
  2. Provide the read check register RData to store the previously read data.

  3. Provides a write check register (WData) to store the last written data.
- Write protection

  All readable and writable registers have write protection function.

5.3 HSTX Interface

5.3.1 Overview of HSTX Interface



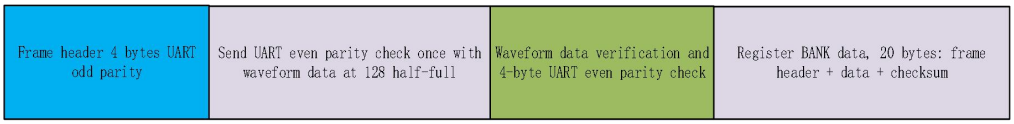
The HSTX interface primarily replaces the UART TX port, using F osc/4 baud rate for active data transmission to the MCU. It supports transmitting waveform data, metering register data, pulse data, and interrupt data.

- The UARTs TX interface is reused for transmitting real-time waveforms at a baud rate of F osc/4.
- Reuse the UARTs TX interface to send pulses and zero-crossing signals.
- Since the UARTs TX port is occupied by the aforementioned solution, the measurement parameters are also periodically transmitted through the TX port.
- Since the UARTs TX pin operates at a different baud rate from the RX pin, the MCU requires two separate UART interfaces with distinct baud rates to interface with the metering chips TX and RX respectively.
- TX actively transmits data including measurement parameters, waveforms, zero-crossing, and pulses.
- The HSTX module can also actively transmit data through the PF/QF/IRQ pins.

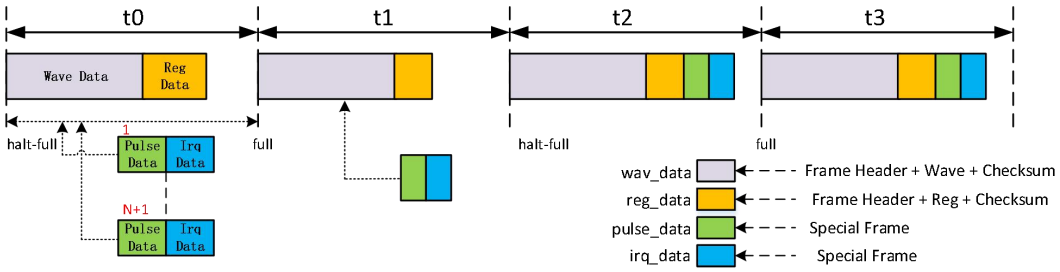
5.3.2 Features of HSTX Interface

- Supports continuous transmission via UART protocol with 8-bit data width.
- The communication baud rate is 1.3824MHz@F osc5.5296MHz, which is 1/4 of the system clock.
- Supports even parity data transmission;
- The data transmission order can be set to high byte first or low byte first.
- The output time of the enabled module can be configured.
- Supports 24-bit/16-bit waveform data transmission.
- Supports metering register transmission in banks (20 bytes)
- Supports three types of pulse data transmission with configurable waiting time.
- Supports interrupt data transmission. When data transmission conflicts occur (i.e., data is being sent simultaneously), you can configure the wait time.
- The length of register data can be configured for each transmission.
- The module output can select from TX/PF/QF/IRQ pins.

5.3.3 HSTX Data Format



The HSTX transmits data in the following formats: waveform data (4-byte frame header with odd parity, data, and 4-byte checksum with even parity) + register data (20 bytes, frame header with odd parity, data, and checksum with even parity) + pulse and interrupt data (4-byte special frame odd parity, with the highest priority inserted at any moment from t0 to t3).



Typical IoT table application format:

1) The voltage channel is configured at 16-bit resolution, while the current channel operates at 24-bit resolution.

2) The typical sampling rate is 21.6k, with 432 samples per cycle at 50Hz. Transmitting a complete dual-channel cycle requires 6–7 half-full cycles.

3) The measurement data comprises: BANK1 (containing valid values, power, frequency, checksum verification, and CRC verification), BANK6 (flag bit), BANK9 (full-wave parameters updated in half cycles), BANK10 (fundamental wave parameters updated in half cycles), and BANK11 (IIC interface temperature sensor data).

4) Set to send 2 BANK measurement parameters at half full capacity each time;

Measurement parameter channel allocation	Bank1 Bank9	Bank2 Bank10	Bank6 Bank9	Bankl1 Bank10	Bank1 Bank9	Bank2 Bank10	Bank6 Bank9	Bank11 Bank10

Waveform data	64-point U 64-point I	64-point U 64-point I	64-point U 64-point I	64-point U 64-point I	64-point U 64-point I	64-point U 64-point I	64-point U 64-point I	64-point U 64-point I
Send interval	2.96ms	2.96ms	2.96ms	2.96ms	2.96ms	2.96ms	2.96ms	2.96ms

Waveform data

The waveform buffer has a capacity of 256×20. The system supports three waveform channels, though most applications typically buffer only one or two channels. The original data is 20 bits, which can be expanded to 24 bits or compressed to 16 bits during transmission, using parity checking. During expansion, special characters are inserted into the lower 4 bits. The U-channel data is defined as {cnt[1:0],0, 1}, the IA-channel data as {cnt[1:0],1, 0}, and the IB-channel data as {cnt[1:0],1, 1}. Here, "cnt" refers to a 0/1/2/3-cycle cyclic counter, with each channel counting independently. The lower 4 bits enable the MCU to identify channels and detect data continuity. This mechanism also prevents ADC sampling data from ever containing five consecutive zero bytes. For 16-bit waveform transmission, the top and bottom 2 bits of the waveform data are compressed before sending.

When the HSTX module is enabled, it transmits half a block of SRAM waveform data each time the waveform buffer reaches half full. The transmission process begins with a 4-byte frame header, where each byte uses odd parity. The header structure consists of: 0x68,0x31, a 1-byte cycle sequence number, and a 1-byte data length (calculated in words, including both waveform and pulse data). By combining the header with received waveform data, the MCU can verify the waveform datas correctness and continuity. After completing the waveform data transmission, a 4-byte checksum (calculated solely for waveform data) is sent to enable data verification by the receiver.

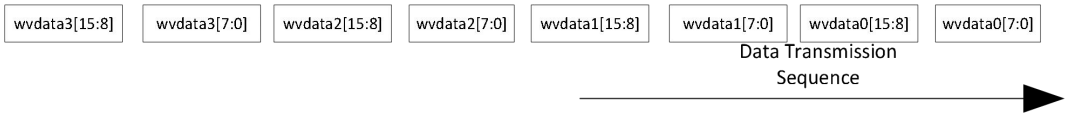
Invert the word count:

The word-based checksum design follows this principle: data is first placed in the lower byte, then accumulated to complete a 32-bit word. After accumulation, the bits are inverted. The frame header is excluded from checksum calculation.

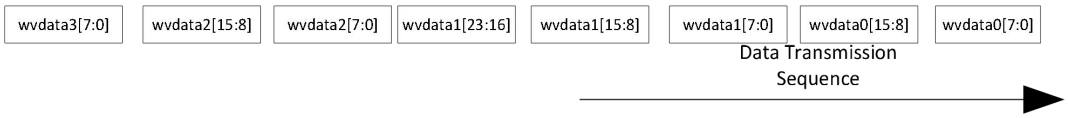
The diagram below illustrates the low-byte-first transmission pattern for single-channel 16-bit waveform data. When configured to compute checksum via word accumulation and inversion, the process involves grouping data into multiple words according to transmission sequence, then performing cumulative inversion. The calculation formula is as follows:

Chksum[31:0]=~

（ {wvdata1[15:8],wvdata1[7:0],wvdata0[15:8],wvdata0[7:0]}+{wvdata3[15:8],wvdata3[7:0], wvdata2[15:8],wvdata2[7:0]}+……）



The diagram below illustrates a dual-channel cross-waveform buffer, where the HSTX configuration features one 16-bit output channel and one 24-bit output channel, with low-byte priority. The schematic diagram of HSTX waveform data transmission is shown below:



The checksum calculation formula is as follows:

Chksum[31:0]=

（ {wvdata1[15:8],wvdata1[7:0],wvdata0[15:8],wvdata0[7:0]}+{wvdata3[7:0],wvdata2[15:8], wvdata2[7:0],wvdata1[23:16]}+……）

Invert by byte accumulation:

If configured to calculate the waveform data checksum by byte accumulation and inversion, all waveform data will be accumulated byte by byte, and the checksum result will be obtained by inversion after accumulation. The result is 32-bit.

measurement register data

The HSTX module organizes all measurement registers in the single-phase chip into 10 banks, each containing 20 bytes of data. The bank allocation is detailed in the table below. The frame header uses odd parity, while the remaining bytes employ even parity.

register address	name	Read and write properties	Register byte count	content	
	frame header	R	1	B1H	BANK120 bytes required for State Grid Version 21 application
22H	IARMS	R	3	xxxxxx	
23H	IBRMS	R	3	xxxxxx	
24H	URMS	R	3	xxxxxx	
25H	UFreq	R	2	xxxx	
26H	PowerPA	R	4	xxxxxxxx	
2DH	EMUStatus	R	3	xxxxxx	
	check sum	R	1	checksum of all data in the BANK	
	frame header	R	1	B2H	BANK220-byte State Grid Version 21 application upper section must
27H	PowerPB	R	4	xxxxxxxx	
28H	PowerQ	R	4	xxxxxxxx	
36H	PowerQB	R	4	xxxxxxxx	
2EH	EMUStatus2	R	3	EMUStatus2	
7FH	DeviceID	R	3	820900	
	check sum	R	1	checksum of all data in the BANK	

	frame header	R	1	B3H	BANK320 bytes bidirectional metering time required
	address	R	1	29H	
29H	EnergyP	R	3	xxxxxx	
	address	R	1	2BH	
2BH	EnergyD	R	3	xxxxxx	
	address	R	1	2AH	
2AH	EnergyP2	R	3	xxxxxx	
	address	R	1	2CH	
2CH	EnergyD2	R	3	xxxxxx	
	continue to have	R	2	Fill in xxx1H	
	check sum	R	1	checksum of all data in the BANK	
	frame header	R	1	B4	BANK420-byte fundamental wave measurement and frozen energy requirement
	address	R	1	37H	
37H	Energy3	R	3	xxxxxx	
	address	R	1	38H	
38H	Energy4	R	3	xxxxxx	
	address	R	1	39H	
39H	Energy5	R	3	xxxxxx	
	address	R	1	3AH	
3AH	Energy6	R	3	xxxxxx	
	continue to have	R	2	Fill in 0001H	
	check sum	R	1	checksum of all data in the BANK	
	frame header	R	1	B5	BANK520-byte fundamental wave measurement and frozen energy requirement
	address	R	1	3BH	
3BH	Energy7	R	3	xxxxxx	
	address	R	1	3CH	
3CH	Energy8	R	3	xxxxxx	
	address	R	1	3DH	
3DH	Energy9	R	3	xxxxxx	
	address	R	1	35H	
35H	UFreq2	R	3	xxxxxx	
	continue to have	R	2	Fill in 0001H	
	check sum	R	1	checksum of all data in the BANK	
	frame header	R	1	B6	BANK620-byt

76H	HW_IBTH	R	3	xxxxxx	e status register, which must be cleared after reading, and leakage-related registers
2FH	EMUStatus3	R	4	xxxxxxxx	
41H	IF	R	1	x	
42H	RIF	R	1	x	
43H	SysStatus	R	1	x	
20H	PFcnt	R/W	2	xxxx	
30H (Extended)	IBDET_CFG	R/W	1	xx	
21H	DFcnt	R/W	2	xxxx	
31H (Extended)	IBDET_FLG	R/W	1	xx	
3EH	PFcnt3	R/W	2	xxxx	
	check sum	R	1	checksum of all data in the BANK	
	frame header	R	1	B7	BANK720-byte fast pulse register, not essential
	address	R	1	3FH	
3FH	PFcnt4	R/W	2	xxxx	
	address	R	1	48H	
48H	PFcnt5	R/W	2	xxxx	
	address	R	1	49H	
49H	PFcnt6	R/W	2	xxxx	
	address	R	1	4AH	
4AH	PFcnt7	R/W	2	xxxx	
	address	R	1	4BH	
4BH	PFcnt8	R/W	2	xxxx	
	address	R	1	4CH	
4CH	PFcnt9	R/W	2	xxxx	
	check sum	R	1	checksum of all data in the BANK	
	frame header	R	1	B9	BANK920 bytes full-wave correlation, half-cycle update
4DH	HW_PA	R	4	xxxxxxxx	
4EH	HW_QA	R	4	xxxxxxxx	
4FH	HW_IA	R	3	xxxxxx	
77H	HW_IB	R	3	xxxxxx	
78H	HW_U	R	3	xxxxxx	
46H	WAVE_IF	RWC	1	x	
	check sum	R	1	checksum of all data in the BANK	
	frame header	R	1	BA	BANK1020 bytes related to
7AH	HW_FI	R	3	xxxxxx	

7BH	HW_FP	R	4	xxxxxxxx	the fundamental wave, half Periodic update or periodic refresh
79H	HW_FU	R	3	xxxxxx	
7CH	SPL_FU	R	4	xxxxxxxx	
7DH	SPL_FI	R	4	xxxxxxxx	
	check sum	R	1	checksum of all data in the BANK	
		amount to	20		
	frame header	R	1	BB	BANK11 IIC module related registers
01H (Extended)	IIC_CTRL	R	2	x xxx	
02H (Extended)	IIC_STA	R	2	x xxx	
03H (Extended)	IIC_SADDR	R	2	x xxx	
04H (Extended)	IIC_TRDAT0	R	2	x xxx	
05H (Extended)	IIC_TRDAT1	R	2	x xxx	
06H (Extended)	IIC_TRDAT2	R	2	x xxx	
07H (Extended)	IIC_TRDAT3	R	2	0x0001	
08H (Extended)	IIC_TRDAT4	R	2	0x0001	
09H (Extended)	IIC_TRDAT5	R	3	0x0001	
	check sum	R	1	checksum of all data in the BANK	
		amount to	20		

Bank 8 retains the bank designation with a zero value, automatically enabling output to maintain the total data volume for each cycle time. Each other bank has an independent output enable bit to control readout. After waveform data output, you can select to output 0, 1, or 2 bank meter register data.

Bank 9 and Bank 10 are half-wave update registers. When enabled, they must send data once per half-wave period, with Bank 9 having the highest priority. The remaining banks transmit data in sequence after enabling.

The checksum for each bank is calculated by summing all byte values of the bank data (including frame header, address, and padding values) and then taking the bitwise complement.

Additionally, register data can be configured to send in low byte/high byte order. This configuration applies only to register data within the bank, but not to the frame header, address, or padding values.

pulse data

The pulse data consists of 4 bytes with a generation cycle of 1 pulse per 10ms, or up to 1 pulse per millisecond in the fastest scenario. Three pulse data types are available: PF, QF, and FPF. To prevent data confusion, a four-byte fixed identifier (which does not overlap with processed parameter register or waveform data, with the last byte serving as a checksum) is used to represent the pulse signal output. Each byte is appended with an odd parity check code to enhance distinguishability.

The interrupt data is 4 bytes long, indicating that the internal interrupt signal is active. Similar to the pulse data, the interrupt data consists of a fixed 4-byte sequence that does not overlap with the processed parameter register data or waveform data. Each byte is appended with an odd parity check code to enhance distinguishability.

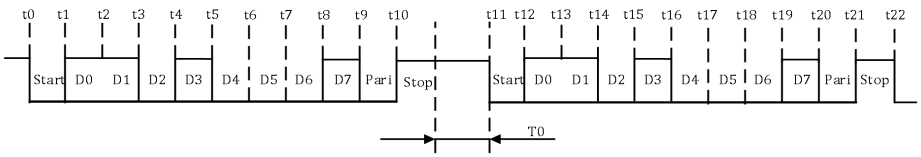
The pulse/interrupt data output details are shown in the figure below (these values can be configured via registers, with the default values listed in the table below):

pulse pattern	Data 0	Data 1	Data 2	Data 3
PF	80H	0AH	20H	AAH
QF	80H	0CH	40H	CCH
FPF	80H	0EH	60H	EEH
IRQ	80H	08H	20H	A8H

To maintain consistent pulse cycles, the system waits 12.292 microseconds (byte transmission time) or 49.168 microseconds (word transmission time) after each pulse generation before transmitting pulse data. During this waiting period, the HSTX module remains idle until the current byte/word data transmission is completed, during which it does not receive new data. Once the waiting period ends, pulse data transmission resumes. After completing pulse data transmission, the HSTX module restarts data reception.

The priority order of the three pulses is PF>QF>FPF>IRQ. When all three pulses and interrupts arrive simultaneously, the PF data is sent first, followed by the interrupt data.

5.3.4 HSTX Frame Format



The diagram illustrates the continuous data transmission of the HSTX module across two consecutive frames. Consistent with the 8-bit UART communication protocol, each frame comprises a START bit, 8-bit data, a parity bit (PARI), and a STOP bit. The frame interval T0 is ≥0, with T0 = 0 during continuous transmission (e.g., waveform data or register output). As shown, the HSTX interface requires 11 bits to transmit a single byte of data including protocol overhead. At a baud rate of 894886, this translates to a transmission time of 0.0123ms per byte.

5.3.5 HSTX Related Registers

See 2.13.6 Extended Register

5.3.6 HSTX Application Process

- Initialize the UART module of the measurement chip and set the baud rate.
- Initialize the UART interface function of the MCU chip, configure the communication baud rate of the UART interface, and establish communication with the metering chip.
- The MCU chip reads the metering configuration register information through the UART interface to check whether the metering chip is operating normally.
- The MCU chip configures the measurement chip via the UART interface to enable waveform buffering.

  Using the UART interface, sequentially write 0xea, 0x87,1<<6|6, and chksum (to initialize the waveform buffer, enable continuous buffering, and configure the U/IB channels).
- The MCU chip configures the HSTX module via UART to control registers, enabling metering registers as needed, setting the HSTX output data format, and activating the HSTX module to switch the metering chips TX function to HSTX mode. It then reads parameters from the metering chips register or the HSTX modules control register through the UART interface to verify successful configuration.

  HSTX->HSTXCtl=1<<16|2<<14|20<<8|1<<6|1; // outputs two Banks when half full, one Bank when full, with data transmission starting 20ms after activation. The IB channel waveform data is output in 24-bit, with high byte data sent first.

  HSTX->HSTX_REG_OE=0x7; //Enable BANK1, BANK2, and BANK3

  HSTX->HSTX_EN=1；

  HSTX->HSTX_LSTX_TXOUT=1；
- The MCU chip sets the UART communication baud rate to Fosc/4 and enables the UART-DMA function.
- The MCU chip configures the UART module in UART_CF mode, enabling the corresponding pulse data interrupt and timeout.
- The measurement chip starts to send the parameter register data, waveform data and interrupt pulse data by using Fosc / 4 baud rate through TX pin.
- The MCU chip receives and processes data, evaluates the single-phase chips operational status based on the received data, and initiates subsequent actions. The following outlines abnormal conditions and follow-up procedures:

  1)If checksum errors are detected in the measurement parameter register or waveform data, disable the HSTX module. Verify the configuration settings of both the HSTX and waveform buffer modules.
- After the MCU chip completes data reception, it clears the interrupt flag, disables DMA enable, exits UART_CF mode, restores normal UART functionality, configures the baud rate write command for the single-phase chip, and switches the metering chips HSTX function to UART mode.

5.4 IIC Interface

5.4.1 Overview of IIC Interface

The IIC (Integrated Circuit Bus) is a two-wire serial bus designed to connect microcontrollers with peripheral devices. Comprising a serial clock line (SCL) and a serial data line (SDA), this bus operates as a half-duplex communication protocol capable of both data transmission and reception. Data transfer between master and slave devices occurs in 8-bit byte units, with communication initiated by the master device and responded to passively by the slave device.

To meet the market demand for terminal temperature measurement, the single-phase metering chip must be equipped with the capability to communicate with external temperature sensors to obtain terminal temperatures. Therefore, adding an IIC interface enables communication with commonly available temperature sensors on the market.

5.3.2 Features of IIC Interface

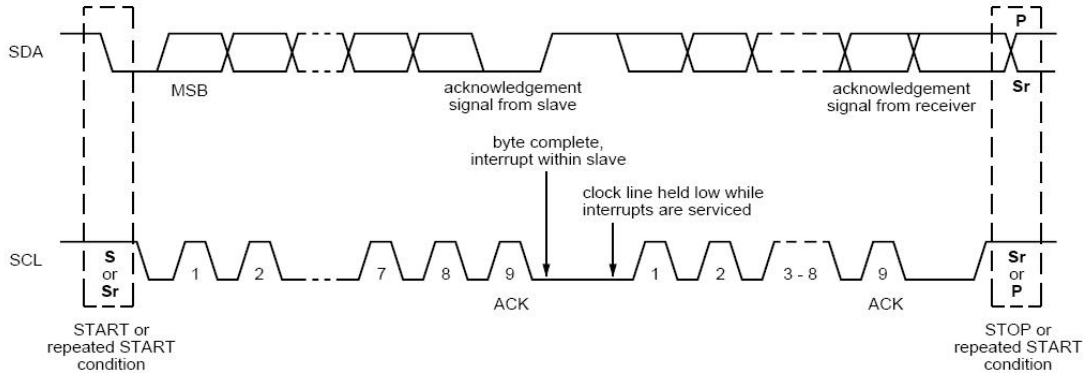
- Uart (Universal Asynchronous Receiver-Transmitter) read/write bus interface
- Select internal pull-up
- Only Master is supported.
- Supports 7-bit address bits;
- Transfer speed: Supports standard mode (100kbps) and high-speed mode (220kbps).
- Supports general mode and dedicated mode;
- The dedicated mode has the following features:
  - The special mode supports four specific sequences: 8bit write, 16bit write, 8bit read, and multi-byte read.
  - Supports multi-byte reading with configurable byte count (i.e., supports adjustable auto-temperature measurement channels: 1~6).
  - Private mode: Supports one-time and automatic sending.
  - The automatic sending mode can be used for automatic temperature measurement mode, and the temperature measurement interval register can be configured.
- The general mode has the following features:
  - Support flexible configuration of start, response, and stop bits.
  - Supported flag queries: transmission completion flag, NACK flag, read/write direction flag

Note: Temperature sensor chips with bus reset functionality are recommended.

5.4.3 IIC Interface General Protocol

The IIC bus consists of two signals: SDA (Serial Data Line) and SCL (Serial Clock Line). A complete IIC transmission comprises four components: the start bit (S), the stop bit (P), the acknowledgment bit (ACK), and the address/data byte. Transmission always begins with the start bit and ends with the stop bit, or restarts with the start bit. Each byte requires a corresponding

acknowledgment bit during transmission.



5.4.4 IIC Interface Specific Timing Specifications

MKE101R supports host mode only and only one master-slave or one master-multiple slave mode (not multi-master mode). It is a dedicated IIC. The general IICs start bit, data transmission bit, response bit, and stop bit are configurable.

The MKE101R supports both Universal Mode and Dedicated Mode. To enable automatic temperature measurement and reduce user intervention, the MKE101R IIC features a dedicated mode that configures specific registers to send tailored sequences. Four sequences are available: 8-bit write, 16-bit write, 8-bit read, and 16-bit read.

Before sending a specific sequence, the user can write the slave device address as needed.

When writing a sequence, the user can only control the slave device address, the slave register address, and the data to be written.

When reading the time sequence, the user can control only the slave device address and the slave register address.

5.4.5 IIC-related registers

See 2.1 5.6 Extended Register

5.3.6 IIC Application Process

Example of Pin Multiplexing

1.Set IIC_CTRL[9:8] to 0 for IIC module configuration to enable internal pull-up for SDA and SCL IO (default value is 0, this step can be omitted).
2.Set the pin function control register 7 (address 0x64) to 0xF0 to enable SDA function on the QF pin.
3.Set the pin function control register 7 (address 0x64) to 0xFE, enabling the PF pin to function as SCL.
4.Then the IIC module can be used normally.

General Mode Example

initialise ：

1. Set IIC_CFG.SP_MODE to 0 for general mode; set IIC_CFG.CLKDIV to select the IIC transmission rate; set IIC_CFG.IIC_EN to 1 to enable IIC.

transmit by radio ：

1. Configure the IIC_SADDR and SM_ADDR registers to set the slave device address and host read/write direction control bits.
2. Set IIC_CTRL.BUSCON=01 to generate the start bit.
3. Read RX_NACK and TRANC, then wait for transmission completion.
4. Configure the TRDAT0[7:0] register to select the slave register address to read.
5. Read RX_NACK and TRANC, then wait for transmission completion.
6. Configure the TRDAT[7:0] register with the data to be sent.
7. Read RX_NACK and TRANC, then wait for transmission completion.
8. Set IIC_CTRL.BUSCON=10: Generate STOP timing

receive ：

1. Configure the IIC_SADDR and SM_ADDR registers to set the slave device address and host write direction control bit.
2. Set IIC_CTRL.BUSCON=01 to generate the start bit.
3. Read RX_NACK and TRANC, then wait for transmission completion.
4. Configure the TRDAT0[7:0] register to select the slave register address to read.
5. Read RX_NACK and TRANC, then wait for transmission completion.
6. Configure the IIC_SADDR and SM_ADDR registers to set the slave device address and host read direction control bit.
7. Set IIC_CTRL.BUSCON=01 to generate the start bit.
8. Read RX_NACK and TRANC, wait for transmission completion without clearing the flag;
9. Configure IIC_CTRL.ACK to determine whether to generate an ACK signal upon receiving the ninth SCL.
10. Clear the TRANC flag, then read RX_NACK and TRANC, wait for the receive to complete. If only 1byte is received, proceed to step 15.
11. Configure IIC_CTRL.ACK to determine whether to generate an ACK signal upon receiving the ninth SCL.
12. Configure IIC_CTRL..RX_SCL_KICK to initiate transmission of 9 SCLs.
13. Read RX_NACK and TRANC, then wait for the reception to complete.
14. Repeat steps 11 to 13 as needed.
15. Set IIC_CTRL.BUSCON=10: Generate STOP timing

Exclusive Mode Example

initialise ：

1. Set IIC_CFG.SP_MODE to 1 for dedicated mode; configure IIC_CFG.CLKDIV to select IICs transmission rate; and set IIC_CFG.IIC_EN to 1 to enable IIC.

Single mode:

Write operation sequence

1. Configure the TRDAT register to set the data to be sent.
2. Configure the IIC_SADDR.SR_ADDR register to set the slave device address, and configure the IIC_SADDR.SM_ADDR register to set the slave device address. (Note: SM_ADDR[0] must be fixed to 0.)
3. Configure IIC_CFG.CMDM to set the transmission timing mode to either 01 (16-bit write) or 00 (8-bit write), and set IIC_CTRL.ONCE_KICK to 1.

Parameters in the same register can be configured simultaneously, meaning you can set all parameters in one IICCTL write operation.

read operation sequence

1. Configure the IIC_SADDR.SR_ADDR register to set the slave device address, and configure the IIC_SADDR.SM_ADDR register to set the slave device address. (Note: SM_ADDR[0] must be fixed to 0.)
2. Configure IIC_CTRL1.CMDM to set the transmission timing mode to either 10 (8-bit read) or 11 (multi-byte read), and set INN_CTRL.ONCE_KICK to 1.
3. Configure IIC_CTRL1.BYTNUM, select the number of bytes to read;
4. When IIC_STA.TRANC reads 1, the IIC is ready to receive the temperature measurement result.
5. To obtain the temperature value, the UART port reads the TRDATx register.

Note: A single read command retrieves the temperature value of a specific channel, determined by the user-configured IIC_SADDR.SM_ADDR register.

automatic mode ：

1. Configure the IIC_SADDR.SR_ADDR register to set the slave device address, and configure the IIC_SADDR.SM_ADDR register to set the slave device address.
2. Configure IIC_CFG.BYTNUM to set the number of bytes to read.
3. Configure IIC_CFG.CMDM to set the transmission timing mode to 11 (multi-byte read), and set IIC_CFG.AUTO=1 to enable auto mode.
4. The received temperature value is stored in the TRDATx register, and the hardware automatically updates the value to bank11.

pay attention to ：

Single-channel automatic temperature measurement must meet the following conditions:

1. If the temperature measurement results of the sensor chip are placed in two registers, the two registers must support multi-byte read function.

If the temperature measurement results are stored in a single register, multi-byte reading may not be supported.

Multi-channel automatic temperature measurement must meet the following conditions:

1. The sensor chip must support multi-byte read timing, or at least the temperature register must support multi-byte read.
2. Temperature measurements from all channels (1 to 6) must be stored in consecutive register addresses.

Example of uploading IIC data via HSTX

General Mode:

The system supports reading from multiple channels, with a maximum of 5 channels. The data is sequentially stored in IIC_TRDAT1[15:0], IIC_TRDAT2[15:0], IIC_TRDAT3[15:0], IIC_TRDAT4[15:0], and IIC_TRDAT5[15:0]. (Note: This feature requires the temperature sensor chip to support continuous reading, and temperature results are stored in consecutive register addresses.)

1. Configure the IIC_SADDR and SM_ADDR registers to set the slave device address and host read/write direction control bits.
2. Set IIC_CTRL.BUSCON=01 to generate the start bit.
3. Waiting for the send to complete;
4. Configure the TRDAT0[7:0] register to select the slave register address to read.
5. Waiting for the send to complete;
6. Configure the IIC_SADDR and SR_ADDR registers to set the slave address and master read/write direction control bits.
7. Set IIC_CTRL.BUSCON=01 to generate the start bit.
8. Wait for the message to be sent without clearing the flag.
9. Configure IIC_CTRL.ACK to determine whether to generate an ACK signal upon receiving the ninth SCL.
10. Clear the flag and wait for transmission completion. If only 1 byte is received, proceed to step 14.
11. Configure IIC_CTRL.ACK to determine whether to generate an ACK signal upon receiving the ninth SCL.
12. Configure IIC_CTRL..RX_SCL_KICK to initiate transmission of 9 SCLs
13. Repeat steps 11-12 based on the number of bytes to receive. Note that the maximum number of bytes read cannot exceed 10 bytes. Exceeding 10 bytes will result in an error in the received data.
14. Set IIC_CTRL.BUSCON=10: Generate STOP timing

Private mode:

The system supports configuring single-channel read operations for up to 6 channels. The read data is sequentially stored in IIC_TRDAT0[15:0].
In IIC_TRDAT1[15:0], IIC_TRDAT2[15:0], IIC_TRDAT3[15:0], IIC_TRDAT4[15:0], and IIC_TRDAT5[15:0] (Note: This function requires the temperature sensor chip to support continuous reading, and the temperature results are stored in consecutive register addresses).

Master single test ：

1.Start a multi-byte read operation.
2.The read data are sequentially stored in the IIC_TRDAT0[15:0], IIC_TRDAT1[15:0], IIC_TRDAT2[15:0], IIC_TRDAT3[15:0], IIC_TRDAT4[15:0], and IIC_TRDAT5[15:0] registers.
3.Wait until the upload of HSTX is complete.
4.Repeat steps 1 through 3

voluntarily ：

1.Configure the auto mode, where HSTX initiates multi-byte read operations.

2.The read data are sequentially stored in the IIC_TRDAT0[15:0], IIC_TRDAT1[15:0], IIC_TRDAT2[15:0], IIC_TRDAT3[15:0], IIC_TRDAT4[15:0], and IIC_TRDAT5[15:0] registers.

The entire temperature measurement process is fully automated, eliminating the need for software intervention.

6 Electrical Characteristics

measuring accuracy

Unless otherwise specified, standard test conditions: DVDD and AVDD are 3.3V or 5V, and TA is 25°C.

parameter	Test Conditions/Notes	least value	representative value	crest value	unit
error of electric energy measurement in fire line have rendered great service idle	 Dynamic range of 20000:1 Dynamic range of 20000:1	 -0.1 -0.1		 +0.1 +0.1	 % %
error of neutral line electric energy measurement have rendered great service idle	 8000:1 dynamic range 8000:1 dynamic range	 -0.1 -0.1		 +0.1 +0.1	 % %
effective value measurement IARMS IBRMS URMS	 Dynamic range of 2000:1 1000:1 dynamic range 1000:1 dynamic range	 -0.1 -0.1 -0.1		 +0.1 +0.1 +0.1	 % % %
bandwidth of electric energy measurement	F_{OSC}=3.579545MHz		7		kHz
frequency measurement scope resolution ratio	 32 Hz, 50Hz frequency measurement 4/8/16 Frequency measurement at 50Hz	 1	 0.001 0.01	 250	 Hz Hz Hz
pulse width of output	high level		90		ms
power supply rejection ratio DC PSRR AC PSRR	 DVDD=AVDD=4.5V~5.0V DVDD=AVDD=2.97V~3.63V 0~80MHz；200mVpp	 -0.15 -0.07		 0.16 0.06 0.01	 % % %

ADC parameter

Unless otherwise specified, standard test conditions: DVDD=AVDD=5V, TA=25°C

parameter	Test Conditions/Notes	least value	representative value	crest value	unit
PGA Gain Selection IA IB/U	 PGA=4、8、12、16、24、32 PGA=1、2、4	 4 1	 16	 32 4	 V/V V/V
Full-scale swing (VxP-VxN) IA/IB/U	RMS=0.707V； Vref=1.25V	-1000		+1000	Vpp
DC input impedance IA IB/U	 PGA=16、24、32 PGA=1		 1000 250		 kΩ kΩ
offset IA IB U	 PGA=8 PGA=16 PGA=1 PGA=1		 0.2 0.5 1.2 0.9		 mV mV mV mV
Output bandwidth (-3dB) IA/IB/U	F osc3.579545MHz ADC_CLK=Fosc/2		6.991		kHz
noise-signal ratio （SNR） IA IB/U	 PGA=16 PGA=1		 90 75.4		 dB dB
ADC cross fire IA IB/U	 $f_{(input)}$=50Hz		 -120 -90		 dB dB

reference voltage

Unless otherwise specified, standard test conditions: DVDD=AVDD=5V, TA=25℃

parameter	Test Conditions/Notes	least value	representative value	crest value	unit
voltage reference	TA=25℃; DVDD=AVDD=5V		1.25		V
temperature coefficient	TA=-40℃~85℃ DVDD=AVDD=3.3V/5.0V	5	10	15	ppm/℃
power supply rejection ratio DC PSRR AC PSRR	 DVDD=AVDD=4.5V~5.5V DVDD=AVDD=2.97V~3.63V 0~80MHz； 200mVpp		 ±0.5 ±0.4 ±0.2		 mV mV mV
load capacity	external 1uF+0.1uF capacitor; 3.97V 3.3V 5.0V		 0.75 0.95 2.5		 mA mA mA

	5.5V		3.05		mA
dispersion	TA=25℃; DVDD=AVDD=5V	1.244	1.25	1.256	mV

clock input

Unless otherwise specified, standard test conditions: DVDD and AVDD are 3.3V or 5V, and TA is 25°C.

parameter	**Test Conditions/Notes**	**least value**	**representative value**	**crest value**	**unit**
input clock frequency	CL=10pF~18pF、 ESR=120Ω ESR=80Ω		3.579545 5.5296		MHz
take-off margin	The load capacitance is 15pF~30pF; DVDD=AVDD=2.6V~5.5V; TA=-40℃~+85℃;		5		times

digital logic

Unless otherwise specified, standard test conditions: DVDD and AVDD are 3.3V or 5V, and TA is 25°C.

parameter	**Test Conditions/Notes**	**least value**	**representative value**	**crest value**	**unit**
Maximum SPI clock rate (SCLK)	t1> 2.3us (see Figure 4-2 for the definition of t1); F_{OSC}=3.579545MHz			2.8	MHz
UART baud rate tolerance	2400bps@F osc 3.579545MHz 4800bps@F osc 3.579545MHz 9600bps@F osc 3.579545MHz 19200bps@F osc 3.579545MHz	 -4 -4 -4 -4		 +4 +4 +4 +4	 % % % %
TTL logic inputs (RSTN, A0, A1, SDI/RX, SCLK/B0, SCSN/B1) Enter high level, V_{INH} Enter low level, V_{INL}	 DVDD=AVDD=5V DVDD=AVDD=3.3V DVDD=AVDD=5V DVDD=AVDD=3.3V	 2.0 1.5 	 	 0.8 0.6	 V V V V
CMOS logic outputs (PF, QF, SDO, IRQN/ZX) Output high level, V_{OH}	 DVDD=AVDD=3.3V; I_{SOURCE}=5mA I_{SINK}=14mA	 2.97 	 	 0.33	 V V

output low level , V_{OL}					
CMOS logic outputs (PF, QF, SDO, IRQN/ZX) Output high level, V_{OH} output low level , V_{OL}	DVDD=AVDD=5.0V; I_{SOURCE}=9mA I_{SINK}=25mA	4 .5		0 .5	V V

Power Supply Voltage Input and Power Consumption

Unless otherwise specified, standard test conditions: DVDD=AVDD=5V, TA=25℃

parameter	Test Conditions/Notes	least value	representative value	crest value	unit
analog power supply voltage	5.0V±10% application	4.50	5.0	5.5	V
	3.3V±10% application	2.97	3.3	3.63	V
digital power supply voltage	5.0V±10% application	4.50	5.0	5.5	V
	3.3V±10% application	2.97	3.3	3.63	V
power dissipation	DVDD=AVDD=5V;				
I_{AVDD}	GIB channel ADC		3.59		mA
	Enable IB channel ADC		4.00		mA
I_{DVDD}	F_{OSC}=3.579545MHz;		1.29		mA
	F_{OSC}=5.5296MHz;		1.81		mA
	DVDD=AVDD=3.3V;				
I_{AVDD}	GIB channel ADC		3.32		mA
	Enable IB channel ADC		3.72		mA
I_{DVDD}	F_{OSC}=3.579545MHz;		0.68		mA
	F_{OSC}=5.5296MHz;		0.98		mA

absolute rating

parameter	
DVDD to DGND	-0.3V~+7V
AVDD to AGND	-0.3V~+7V
From DGND to AGND	-0.3V~+0.3V
Simulate input to AGND; V1P, V1N, V2P, V2N, V3P, V3N	-6V~+6V
The digital input voltage relative to DGND	-0.3V~DVDD+0.3V
The digital output voltage relative to DGND	-0.3V~DVDD+0.3V
operating temperature range	-40℃~+85℃
storage temperature range	-65℃~150℃
maximum junction temperature	1 50℃

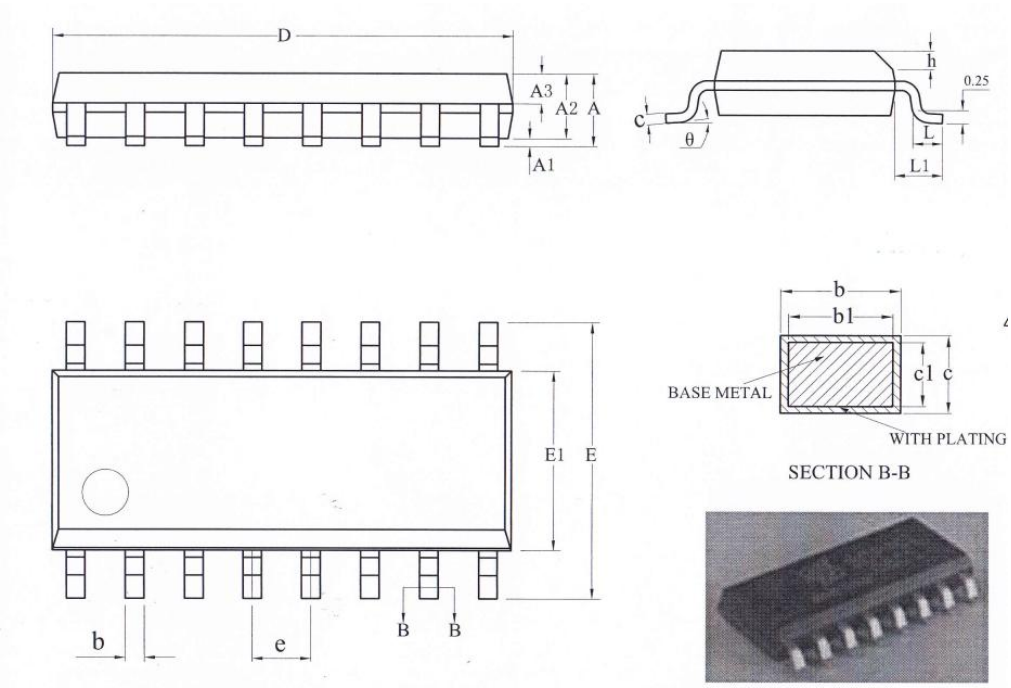
ESD parameter

parameter	Test Conditions/Notes	price	unit
Electrostatic Discharge	Human Body Model (HBM) is tested on all pins in accordance with the standard JEDEC EIA/JESD22-A114.	4500	V

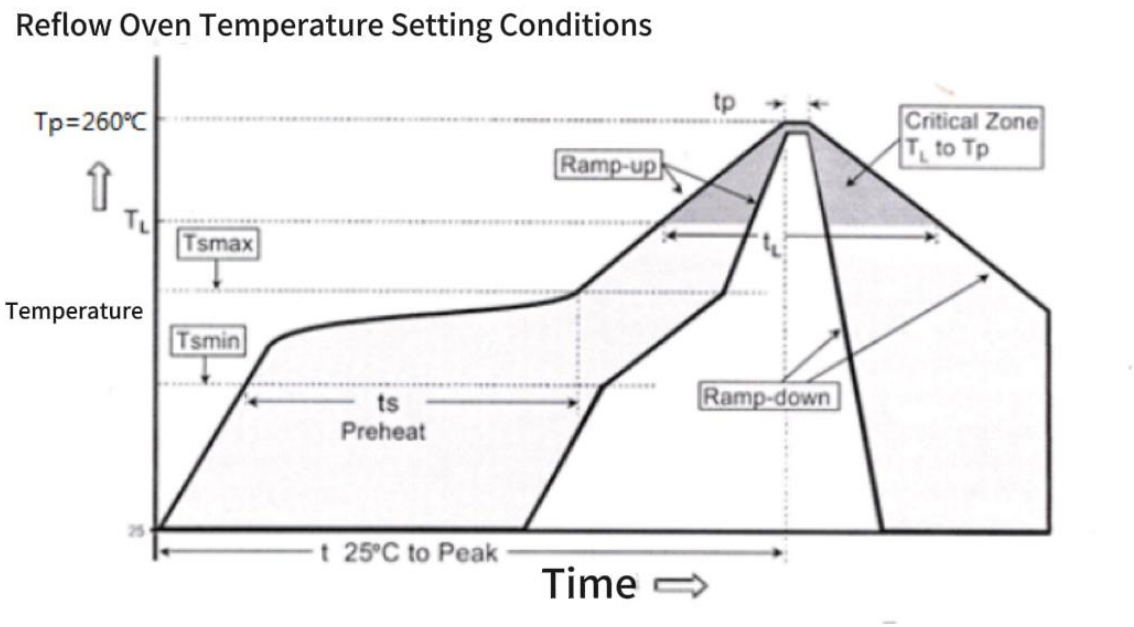
(ESD)	The mechanical model (MM) is tested on all pins in accordance with the standard JEDEC EIA/JESD22-A115C.	400	V
Humidity Sensitivity (MSL)	Evaluation according to the standard IPC/JEDEC J-STD-020D.1	Level 3	/
Latch-up experiment	Perform the procedure on all pins in accordance with JEDEC STANDARD NO.78D (November 2001).	200	mA

7 Chip Packaging and Soldering Conditions

Chip package dimensions of MKE101R-SOP16L:



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	---	---	1.75
A1	0.05	---	0.225
A2	1.30	1.40	1.50
A3	0.6	0.65	0.70
b	0.39	---	0.48
b1	0.38	0.41	0.43
c	0.21	---	0.26
c1	0.19	0.20	0.21
D	9.70	9.90	10.10
E	5.80	6.00	6.20
E1	3.70	3.90	4.10
e	1.27BSC		
h	0.25	---	0.5
L	0. 5	---	0.8
L1	1.05BSC		
θ	0	-----	8°



Temperature Setting Curve of Reflow Soldering Furnace

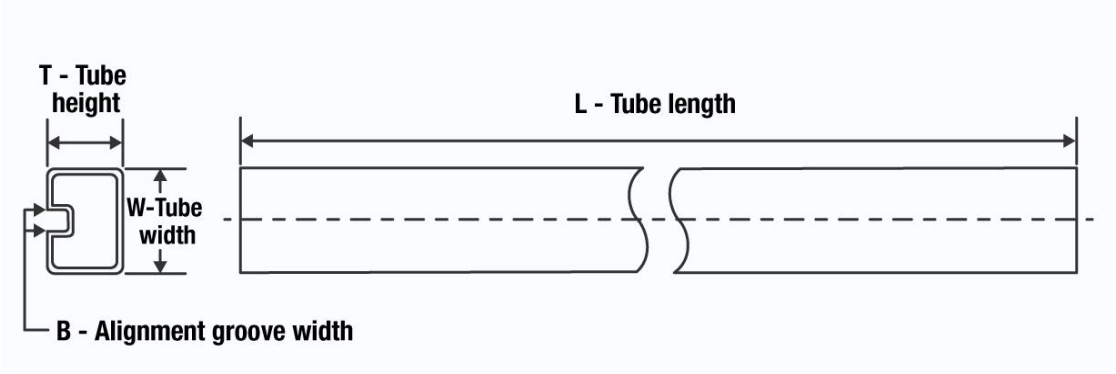
Distribution plot characteristics	price
average slope rate （TL to Tp）	Maximum 3°C/second
preheat Minimum temperature (Ts min) Maximum temperature (Ts max) Time (minimum-maximum) (ts)	 150℃ 200℃ 60-180 seconds
Ts max-TL Inclination rise rate (Ts max to TL)	Maximum 3°C/second
Keep the above time - temperature （TL） - time （tL）	 217℃ 60-150 seconds
Peak temperature (Tp)	260+5/-0℃
Time (tp) within the actual peak temperature of 5°C	20-40 seconds
tilt rate	Maximum 6°C/second
Time from 25°C to peak temperature	Maximum 8 minutes
holding temperature TL peak temperature Tp Average Tilt Rate (TL to Tp)	217℃ 260℃ Maximum 3°C/second

9 Packaging Information

The chip is available in two packaging options: tube and tape, with the specifications as follows.

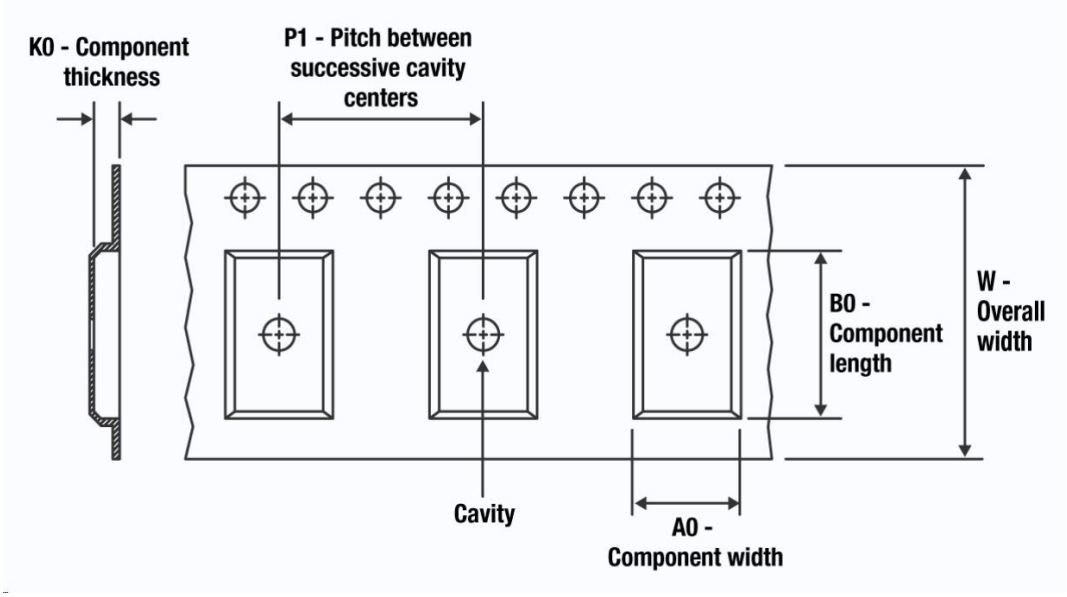
9.1 Material Pipe Specifications

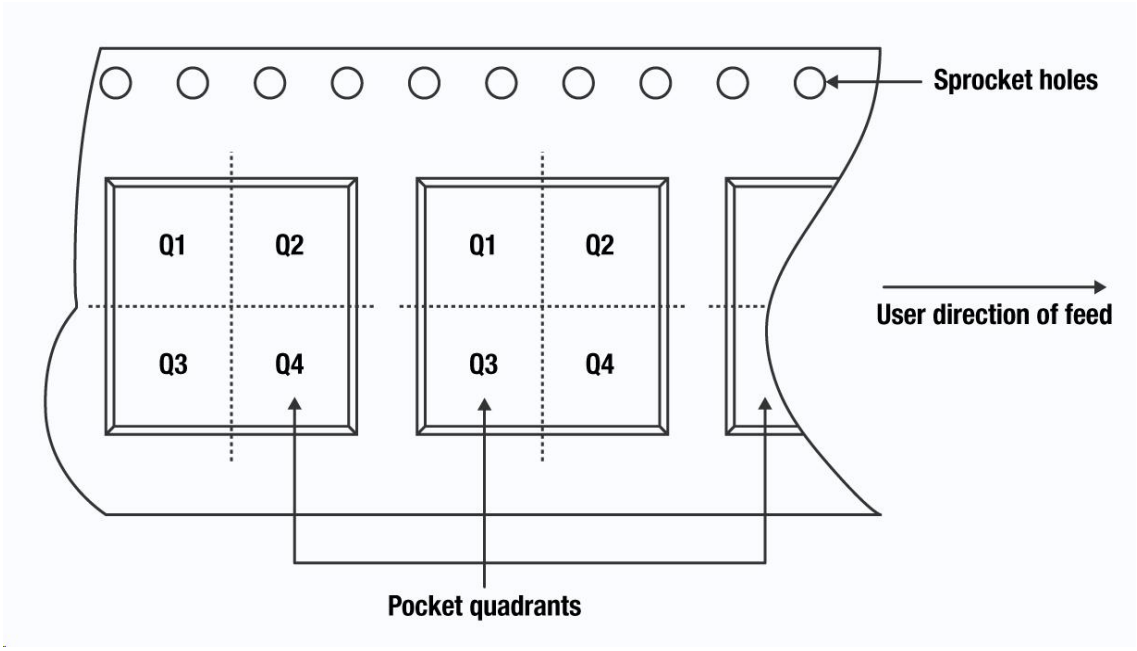
encapsulation form	pipe fitting						
	Quantity per tube	B(mm)	T(mm)	W(mm)	L(mm)	Quantity per box	Quantity per box
SSOP24L	60	5.0±0.15	3.5±0.1	10.8±0.1	520±1.0	10000	60000
SOP16L	50	2.4±0.1	3.4±0.1	7.8±0.1	520±1.0	10000	60000



encapsulation form	braid											
	Quantity per tray	Quantity per box	Spool diameter (mm)	drum width（mm）	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	D0 (mm)	W (mm)	Pin1 quadrant
SOP16L	3000	30000	330±1	16 4±0 2	6 7±0 1	10 4±0 1	2 0±0 1	4 0±0 1	8 0±0 1	1 5+0 1	16 0±0 1	Q1（upper left）
SSOP24L	2000	20000	330±1	16 4±0 2	8 4±0 1	8 7±0 1	2 5±0 1	4 0±0 1	12 0±0 1	1 5+0 1	16 0±0 1	Q1（upper left）

9.2 Tape Specifications




Sprocket holes
Q1
Q2
Q3
Q4
Q1
Q2
Q3
Q4
User direction of feed
Pocket quadrants

Appendix 1: Reactive Power Phase Compensation Table

frequency (Hz)	Phase shift (°)	Phase shift deviation (°)	reactive power accuracy deviation	**Qphs compensation value (Hex)**
45	90.132	-0.132	0.40%	4C
46	90.104	-0.104	0.31%	3C
47	90.076	-0.076	0.23%	2B
48	90.049	-0.049	0.15%	1C
49	90.022	-0.022	0.07%	D
50	89.996	0.004	-0.01%	FFFE
51	89.971	0.029	-0.09%	FFEF
52	89.946	0.054	-0.16%	FFE1
53	89.9227	0.0773	-0.23%	FFD4
54	89.897	0.103	-0.31%	FFC5
55	89.874	0.126	-0.38%	FFB8
56	89.85	0.15	-0.45%	FFAA
57	89.828	0.172	-0.52%	FF9E
58	89.805	0.195	-0.59%	FF91
59	89.782	0.218	-0.66%	FF83
60	89.761	0.239	-0.72%	FF77
61	89.739	0.261	-0.79%	FF6B
62	89.717	0.283	-0.85%	FF5E
63	89.696	0.304	-0.92%	FF52
64	89.676	0.324	-0.98%	FF47
65	89.655	0.345	-1.04%	FF3B