MKE101R
DataSheet

Rev 1.0

Revision Histroy

version number	Modification time	revise content
Rev 1.0	2025-02-13	First release

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1 Chip Introduction

The MKE101R, a high-precision and highly reliable single-phase metering chip by MAKSA, is designed for various metering applications including smart meters, energy consumption analysis, power monitoring, and electrical safety.

1.1 Chip Characteristics

- ✓ calculate
  - It provides a three-channel sum-delta ADC, including the voltage channel (U channel), current channel A (IA channel), and current channel B (IB channel).①
  - The IA channel PGA supports 4x,8x,12x,16x (default), 24x, and 32x amplification, but not 1x or 2x. The IB and U channel PGA support 1x,2x, and 4x amplification.②
  - The active power metering performance of the front line (A line) shows a nonlinear error of <0.1% within a dynamic range of 20000:1.③
  - The reactive power metering performance of the line maintains a non-linear error below 0.1% within a dynamic range of 20000:1.
  - It provides three-channel RMS measurement. The IA channel has a dynamic range of 2000:1 with a nonlinearity error <0.1%. The IB and U channels have a dynamic range of 1000:1 with a nonlinearity error <0.1%.
  - Provides two-phase active and reactive power output on the live and neutral lines (B channel), supporting dual-phase active and reactive power metering.
  - A pulse frequency generator is provided for accumulating and integrating electrical energy at user-defined power levels.
  - Provide three-channel ADC instantaneous sampling values and support instantaneous sampling value update interrupts
  - The threshold for latent movement can be adjusted.
  - It provides reverse active power indication and outputs the REVP reverse indication signal through the QF pin.
  - Provide U-channel frequency measurement
  - Provide U-channel zero-crossing detection
  - Supports zero-crossing signals from Ia channels to be output through the TX pin of the UART port.
  - Supports reference voltage monitoring, see VREF_OK
  - Supports bidirectional measurement to meet the requirements for rapid power flow change testing
  - Active power supports both full-wave and fundamental wave metering.
  - reactive power support fundamental wave metering
  - Both active and reactive power support half-wave metering
- ✓ software calibration
  - The meter constant (HFConst) is adjustable.
  - Provide gain and phase correction

- Provide active, reactive, and RMS offset correction
- Provide small signal calibration acceleration function
- Enable automatic configuration parameter validation

✓ Supports arbitrary single-channel, dual-channel, or triple-channel ADC waveform buffering, with continuous waveform acquisition via SPI/UART ports.

✓ The RX input pin of a UART module serves dual functions: global reset (via the pin) and local reset (via the UART module).

✓ Features power monitoring capability

✓ Electric energy register with timing freeze function

✓ Supports synchronous sampling

✓ Supports fast leakage detection

✓ Supports DC detection

✓ Supports voltage and current transient event detection

✓ Supports single-phase three-wire ±P1±P2 and ±Q1±Q2 integration operations

✓ Configure register support for CRC16

✓ Supports adjustable pulse width and level inversion for power

✓ Supports Ia±Ib RMS calculation

✓ Supports asymmetric baud rate UART communication. The TX module features HSTX functionality with a baud rate of Fosc/4 (crystal oscillator frequency). HSTS automatically transmits real-time waveforms, metering parameters, power pulses, interrupts, and other data. The RX baud rate and communication parameters remain unchanged.

✓ Supports IIC host communication for convenient interaction with external temperature sensor chips, used for terminal temperature measurement.

✓ Supports error self-monitoring function

✓ Supports software-adjustable UART baud rate

✓ The MKE101R operates on a +5V/3.3V power supply, with typical power consumption values of

Crystal frequency / Power supply voltage	5V	3.3V
3.579545MHz	2 7mW	15mW
5.5296MHz	30 mW	16 mW

✓ Built-in 1.25V±1% reference voltage, with a typical temperature coefficient of 5ppm/℃ and a maximum of 15ppm/℃.

✓ The MKE101R is packaged in SOP16L green packaging.

① Channel A is called IA channel, channel B is called IB channel, and channel U is called U channel.
② In this article, red text indicates new or upgraded features in V5, which will not be repeated later.
③ The live wire is called A line, and the neutral wire is called B line.

1.2 Function Overview

The MKE101R meter provides comprehensive measurement capabilities for all-wave and fundamental wave active/reactive power, voltage/current RMS values, line frequency, and half-cycle updates of active/reactive power and voltage/current values. It supports dual independent channels for active/reactive power and current RMS values, with full compliance to all current metrology standards including active energy metering, reactive energy metering, fundamental wave metering,

half-wave metering, and bidirectional metering.

The MKE101R features fully digital gain, phase, and offset calibration. Active power pulses are output from the PF/QF/IRQ pins, while reactive power pulses, user-defined power pulses, and REVP can be output from the same pins.

The MKE101R features both SPI and UART serial interfaces, enabling seamless communication with external microcontrollers.

The MKE101R features an IIC host interface for seamless communication with external temperature sensor chips, enabling terminal temperature measurement.

The MKE101R features an HSTX interface (high-speed UART TX interface) that automatically transmits real-time waveforms, measurement parameters, pulses, and other data.

The power monitoring circuit inside MKE101R can ensure the reliable operation of the chip when power is on and off.

1.3 Function Block Diagram

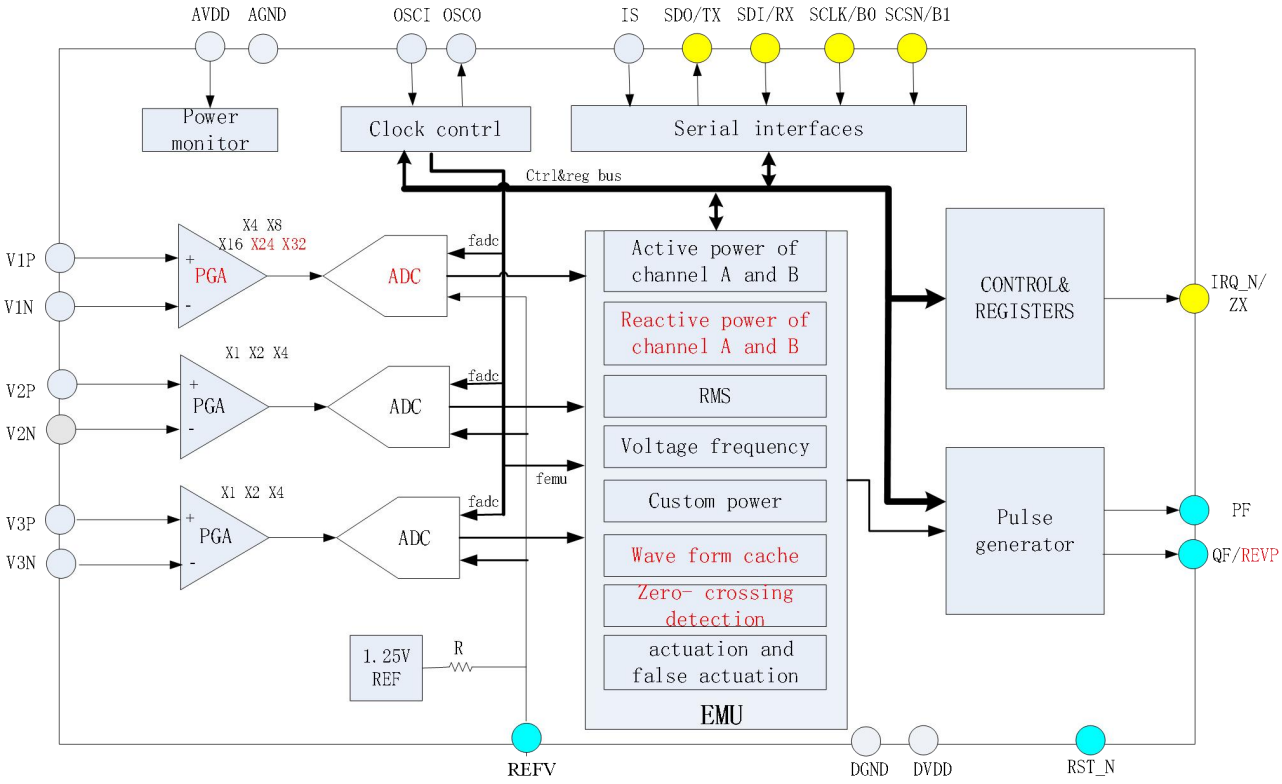


Figure 1-1 Function Block Diagram

1.4 Pin Definitions

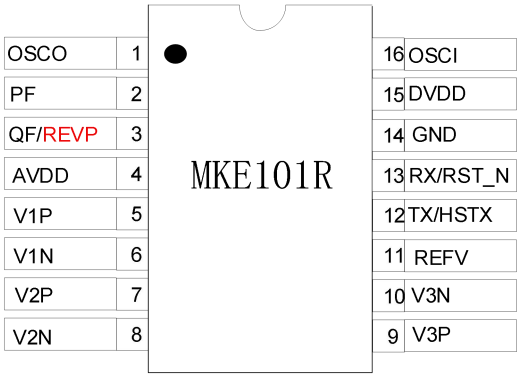


Figure 1-2 Pin layout diagram of MKE101R-SOP16L

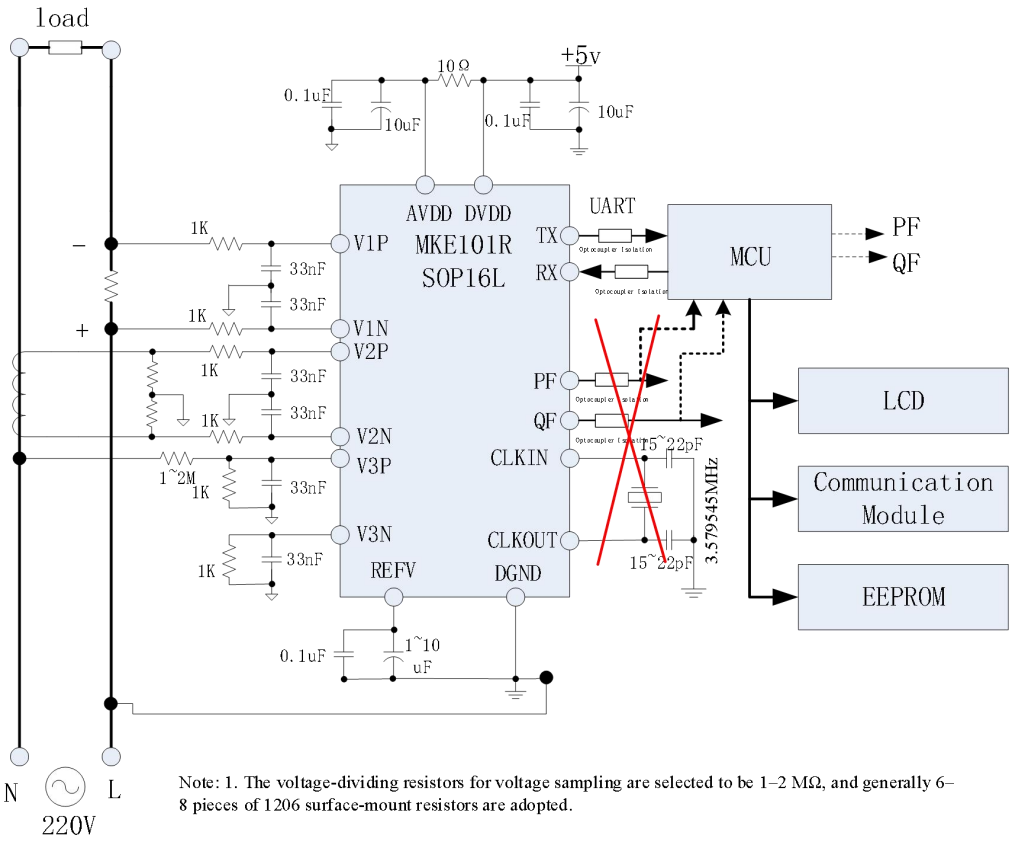
pin	characteristic	characteristic	functional description
1	OSCO	output	The output of the external crystal.
2	PF	output	The active power pulse output defaults to low-level output. Its frequency reflects the instantaneous active power level. It has a 5mA output and current absorption capability.
3	QF/ REVP	output	This pin is a QF/REVP multiplex pin (default QF). When EMUCON2.QFCFG=0, it functions as a QF pin to output either reactive power verification pulses or user-defined pulses, with low-level output as the default. The frequency reflects the magnitude of either reactive power or user-defined power values, which include three options: second active power, sum of two active power vectors, or user-defined power register. It features a 5mA output and current absorption capability. When EMUCON2.QFCFG=1, the REVP pin functions as a negative power indicator.
4	AVDD	source	Analog power pin. This pin supplies power to the analog section of the chip. It should be externally connected with a 10μF capacitor in parallel and a 0.1μF decoupling capacitor. Typical operating voltage range: 2.97V to 5.5V. After selecting a standard supply voltage (e.g., 5V or 3.3V), ensure the power supply fluctuation remains within ±10% of the specified range.
5，6	V1P, V1N	import	The positive and negative analog input pins of the I/O channel. It operates in full differential mode, with a maximum input voltage of ±1000mV and a maximum withstand voltage of ±6V. The external sampling circuit, when performing standard full-wave measurement, requires an anti-aliasing resistance of 1kΩ and an anti-aliasing capacitance ranging from 10nF to 33nF. For harmonic measurement or power quality analysis, the required anti-aliasing resistance is 1kΩ and the anti-aliasing capacitance is 3.3nF.

7，8	V2P, V2N	import	The positive and negative analog input pins of the IB channel. It operates in full differential mode, with a maximum input Vpp of ±1000mV and a maximum withstand voltage of ±6V. The external sampling circuit, when performing standard full-wave measurement, requires an anti-aliasing resistance of 1kΩ and an anti-aliasing capacitance ranging from 10nF to 33nF. For harmonic measurement or power quality analysis, the required anti-aliasing resistance is 1kΩ and the anti-aliasing capacitance is 3.3nF.
9，10	V3P,V3N	import	The U-channel features positive and negative analog input pins. It operates in fully differential mode, with a maximum input voltage of ±1000mV and a maximum withstand voltage of ±6V under normal operation. The external sampling circuit, when performing standard full-wave measurement, requires an anti-aliasing resistance of 1kΩ and an anti-aliasing capacitance ranging from 10nF to 33nF. For harmonic measurement or power quality analysis, the required anti-aliasing resistance is 1kΩ and the anti-aliasing capacitance is 3.3nF.
11	REFV	Input/Output	The input/output pin for the 1.25V reference voltage. The external reference source can be directly connected to this pin. Whether using an internal or external reference source, this pin should be decoupled with a minimum of 1μF capacitor in parallel with a 0.1μF capacitor.
12	TX	output	This pin serves as the TX data output port for UART. Using special commands, it can generate a zero-crossing signal for the IA channel, typically a 10ms square wave. For details, refer to the Special Commands section. The TX function can be reconfigured as HSTX. Operating at baud rates of Fosc/4 (895K@3.579545MHz or 1382K@5.5296MHz), the TX pin automatically transmits real-time waveforms, measurement parameters, pulses, and other data.
13	RX/RST_N	import	This pin serves as both the UART input RX and a reset pin. A local reset (UART module reset) occurs when the low-level input signal persists for between 10ms and 20ms, while a global reset (chip-wide reset) is triggered if the signal remains low for over 20ms. The internal reset circuit of MKE101R is completely independent of the UART communication circuit, and its pin reset function is identical to that of an independent pin reset.
14	GND	the earth	In the chip circuit, ensure this pin is not directly connected to ground points with high digital noise (e.g., DVDD decoupling capacitor), and maintain a sufficient distance from them.
15	DVDD	source	Digital power pin. This pin supplies power to the digital section of the chip. It should be externally connected with a 10μF capacitor in parallel and a 0.1μF decoupling capacitor. Typical operating voltage range: 2.97V to 5.5V. After selecting a standard supply voltage (e.g.,

			5V or 3.3V), ensure the power supply fluctuation remains within ±10% of the specified range.
16	OSCI	import	The input terminal of the external crystal or the clock input of the external clock system. The typical frequency of the external crystal is 3.579545 MHz. The typical value of the external capacitor is 15 pF to 22 pF, and there is already an internal bypass resistance of approximately 4 MΩ, so no external bypass resistor is required. For 3.579545 MHz, the ESR of the external crystal must be less than 120 ohms; for 5.5296 MHz, the ESR must be less than 80 ohms.

1.5 Typical Applications

1.5.1 State Grid Single-Phase 20 Version



Note: 1. The voltage-dividing resistors for voltage sampling are selected to be 1–2 MΩ, and generally 6–8 pieces of 1206 surface-mount resistors are adopted.

Figure 1-5 Typical Applications of State Grid Single-phase Meters

The MKE101R features three Σ-Δ ADC channels. The IA channel ADC (V1P/V1N inputs) uses

live-wire manganized copper for sampling, while the IB channel ADC (V2P/V2N inputs) employs neutral-wire transformer sampling. The U channel ADC (V3P/V3N inputs) handles voltage sampling. The high-performance IA channel ADC has a small manganized copper input signal and defaults to 16x PGA, whereas the IB and U channel ADCs have larger input signals and are configured at 1x PGA by default.

2 Electrical Characteristics

measuring accuracy

Unless otherwise specified, standard test conditions: DVDD and AVDD are 3.3V or 5V, and TA is 25°C.

parameter	Test Conditions/Notes	least value	representative value	crest value	unit
error of electric energy measurement in fire line have rendered great service idle	 Dynamic range of 20000:1 Dynamic range of 20000:1	 -0.1 -0.1		 +0.1 +0.1	 % %
error of neutral line electric energy measurement have rendered great service idle	 8000:1 dynamic range 8000:1 dynamic range	 -0.1 -0.1		 +0.1 +0.1	 % %
effective value measurement IARMS IBRMS URMS	 Dynamic range of 2000:1 1000:1 dynamic range 1000:1 dynamic range	 -0.1 -0.1 -0.1		 +0.1 +0.1 +0.1	 % % %
bandwidth of electric energy measurement	F_{OSC}=3.579545MHz		7		kHz
frequency measurement scope resolution ratio	 32 Hz, 50Hz frequency measurement 4/8/16 Frequency measurement at 50Hz	 1	 0.001 0.01	 250	 Hz Hz Hz
pulse width of output	high level		90		ms
power supply rejection ratio DC PSRR AC PSRR	 DVDD=AVDD=4.5V~5.0V DVDD=AVDD=2.97V~3.63V 0~80MHz；200mVpp	 -0.15 -0.07		 0.16 0.06 0.01	 % % %

ADC parameter

Unless otherwise specified, standard test conditions: DVDD=AVDD=5V, TA=25°C

parameter	Test Conditions/Notes	least	representative	crest	unit

		value	value	value	
PGA Gain Selection IA IB/U	 PGA=4、8、12、16、24、32 PGA=1、2、4	 4 1	 16	 32 4	 V/V V/V
Full-scale swing (VxP-VxN) IA/IB/U	RMS=0.707V；Vref=1.25V	-1000		+1000	Vpp
DC input impedance IA IB/U	 PGA=16、24、32 PGA=1		 1000 250		 kΩ kΩ
offset IA IB U	 PGA=8 PGA=16 PGA=1 PGA=1		 0.2 0.5 1.2 0.9		 mV mV mV mV
Output bandwidth (-3dB) IA/IB/U	F osc3.579545MHz ADC_CLK=Fosc/2		6.991		kHz
noise-signal ratio （SNR） IA IB/U	 PGA=16 PGA=1		 90 75.4		 dB dB
ADC cross fire IA IB/U	 $f_{(input)}$=50Hz		 -120 -90		 dB dB

reference voltage

Unless otherwise specified, standard test conditions: DVDD=AVDD=5V, TA=25℃

parameter	**Test Conditions/Notes**	**least value**	**representative value**	**crest value**	**unit**
voltage reference	TA=25℃; DVDD=AVDD=5V		1.25		V
temperature coefficient	TA=-40℃~85℃ DVDD=AVDD=3.3V/5.0V	5	10	15	ppm/℃
power supply rejection ratio DC PSRR AC PSRR	 DVDD=AVDD=4.5V~5.5V DVDD=AVDD=2.97V~3.63V 0~80MHz；200mVpp		 ±0.5 ±0.4 ±0.2		 mV mV mV
load capacity	external 1uF+0.1uF capacitor; 3.97V 3.3V 5.0V 5.5V		 0.75 0.95 2.5 3.05		 mA mA mA mA

dispersion	TA=25℃; DVDD=AVDD=5V	1.244	1.25	1.256	mV

clock input

Unless otherwise specified, standard test conditions: DVDD and AVDD are 3.3V or 5V, and TA is 25°C.

parameter	**Test Conditions/Notes**	**least value**	**representative value**	**crest value**	**unit**
input clock frequency	CL=10pF~18pF、 ESR=120Ω ESR=80Ω		 3.579545 5.5296		MHz
take-off margin	The load capacitance is 15pF~30pF; DVDD=AVDD=2.6V~5.5V; TA=-40℃~+85℃;		5		times

digital logic

Unless otherwise specified, standard test conditions: DVDD and AVDD are 3.3V or 5V, and TA is 25°C.

parameter	**Test Conditions/Notes**	**least value**	**representative value**	**crest value**	**unit**
Maximum SPI clock rate (SCLK)	t1> 2.3us (see Figure 4-2 for the definition of t1); F_{OSC}=3.579545MHz			2.8	MHz
UART baud rate tolerance	2400bps@F osc 3.579545MHz 4800bps@F osc 3.579545MHz 9600bps@F osc 3.579545MHz 19200bps@F osc 3.579545MHz	 -4 -4 -4 -4		 +4 +4 +4 +4	 % % % %
TTL logic inputs (RSTN, A0, A1, SDI/RX, SCLK/B0, SCSN/B1) Enter high level, V_{INH} Enter low level, V_{INL}	 DVDD=AVDD=5V DVDD=AVDD=3.3V DVDD=AVDD=5V DVDD=AVDD=3.3V	 2.0 1.5		 0.8 0.6	 V V V V
CMOS logic outputs (PF, QF, SDO, IRQN/ZX) Output high level, V_{OH} output low level ,	DVDD=AVDD=3.3V; I_{SOURCE}=5mA I_{SINK}=14mA	 2.97		 0.33	 V V

V_{OL}					
CMOS logic outputs (PF, QF, SDO, IRQN/ZX) Output high level, V_{OH} output low level , V_{OL}	DVDD=AVDD=5.0V; I_{SOURCE}=9mA I_{SINK}=25mA	4 .5		0 .5	V V

Power Supply Voltage Input and Power Consumption

Unless otherwise specified, standard test conditions: DVDD=AVDD=5V, TA=25℃

parameter	Test Conditions/Notes	least value	representative value	crest value	unit
analog power supply voltage	5.0V±10% application	4.50	5.0	5.5	V
	3.3V±10% application	2.97	3.3	3.63	V
digital power supply voltage	5.0V±10% application	4.50	5.0	5.5	V
	3.3V±10% application	2.97	3.3	3.63	V
power dissipation	DVDD=AVDD=5V;				
I_{AVDD}	GIB channel ADC		3.59		mA
	Enable IB channel ADC		4.00		mA
I_{DVDD}	F_{OSC}=3.579545MHz;		1.29		mA
	F_{OSC}=5.5296MHz;		1.81		mA
	DVDD=AVDD=3.3V;				
I_{AVDD}	GIB channel ADC		3.32		mA
	Enable IB channel ADC		3.72		mA
I_{DVDD}	F_{OSC}=3.579545MHz;		0.68		mA
	F_{OSC}=5.5296MHz;		0.98		mA

absolute rating

parameter	
DVDD to DGND	-0.3V~+7V
AVDD to AGND	-0.3V~+7V
From DGND to AGND	-0.3V~+0.3V
Simulate input to AGND; V1P, V1N, V2P, V2N, V3P, V3N	-6V~+6V
The digital input voltage relative to DGND	-0.3V~DVDD+0.3V
The digital output voltage relative to DGND	-0.3V~DVDD+0.3V
operating temperature range	-40℃~+85℃
storage temperature range	-65℃~150℃
maximum junction temperature	150℃

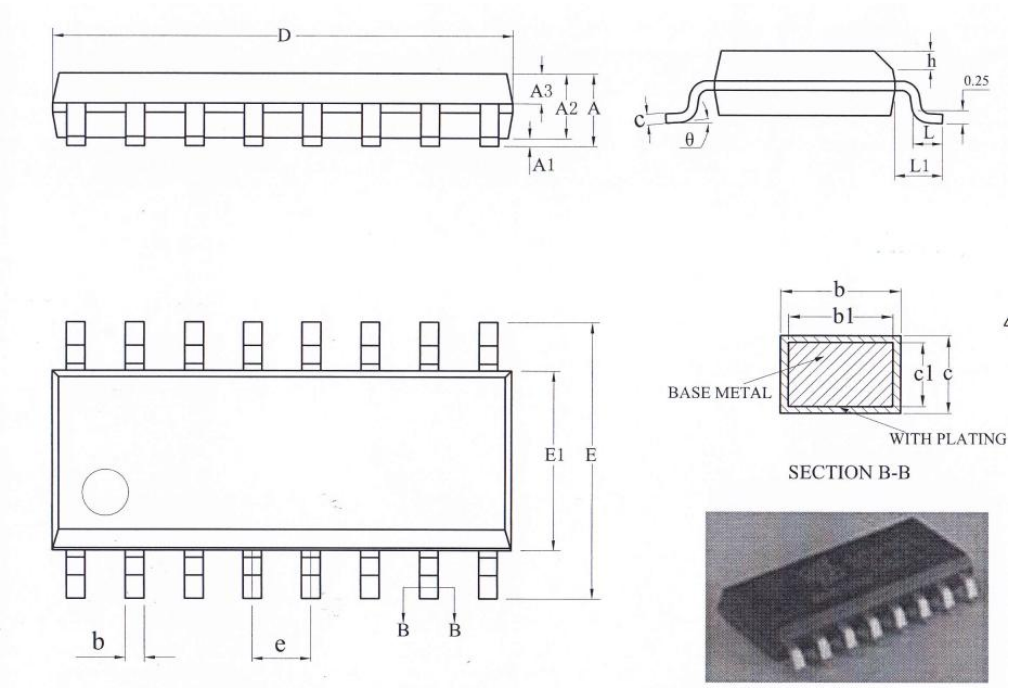
ESD parameter

parameter	Test Conditions/Notes	price	unit
Electrostatic Discharge (ESD)	Human Body Model (HBM) is tested on all pins in accordance with the standard JEDEC EIA/JESD22-A114.	4500	V
	The mechanical model (MM) is tested on all pins in accordance with the standard JEDEC EIA/JESD22-A115C.	400	V

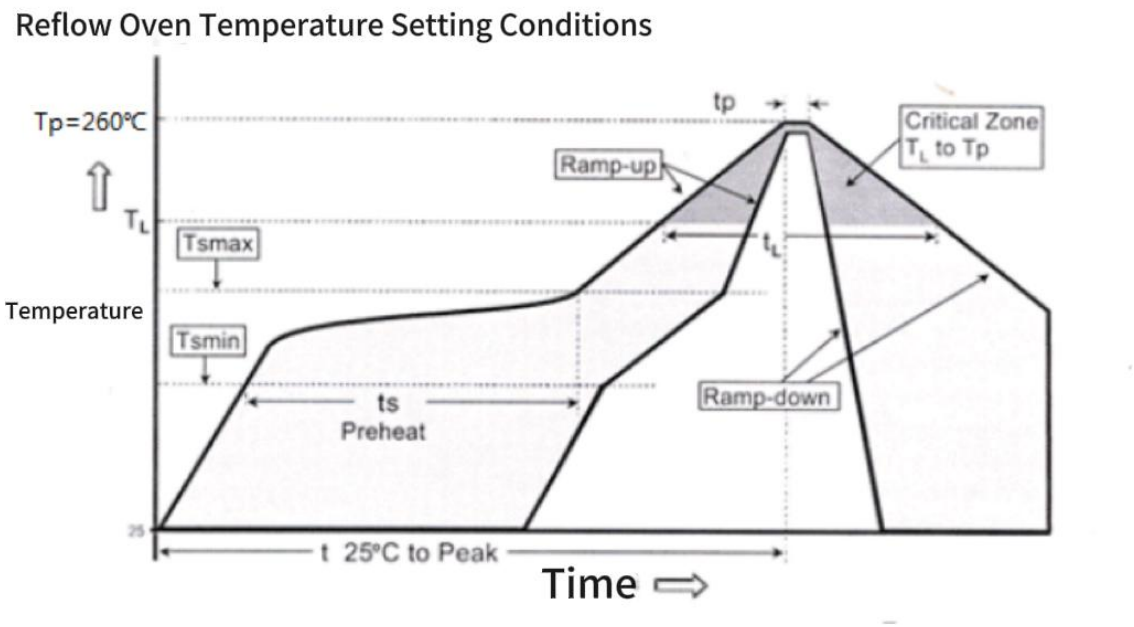
Humidity Sensitivity (MSL)	Evaluation according to the standard IPC/JEDEC J-STD-020D.1	Level 3	/
Latch-up experiment	Perform the procedure on all pins in accordance with JEDEC STANDARD NO.78D (November 2001).	200	mA

3 Chip Packaging and Soldering Conditions

Chip package dimensions of MKE101R-SOP16L:



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	---	---	1.75
A1	0.05	---	0.225
A2	1.30	1.40	1.50
A3	0.6	0.65	0.70
b	0.39	---	0.48
b1	0.38	0.41	0.43
c	0.21	---	0.26
c1	0.19	0.20	0.21
D	9.70	9.90	10.10
E	5.80	6.00	6.20
E1	3.70	3.90	4.10
e	1.27BSC		
h	0.25	---	0.5
L	0. 5	---	0.8
L1	1.05BSC		
θ	0	-----	8º



Temperature Setting Curve of Reflow Soldering Furnace

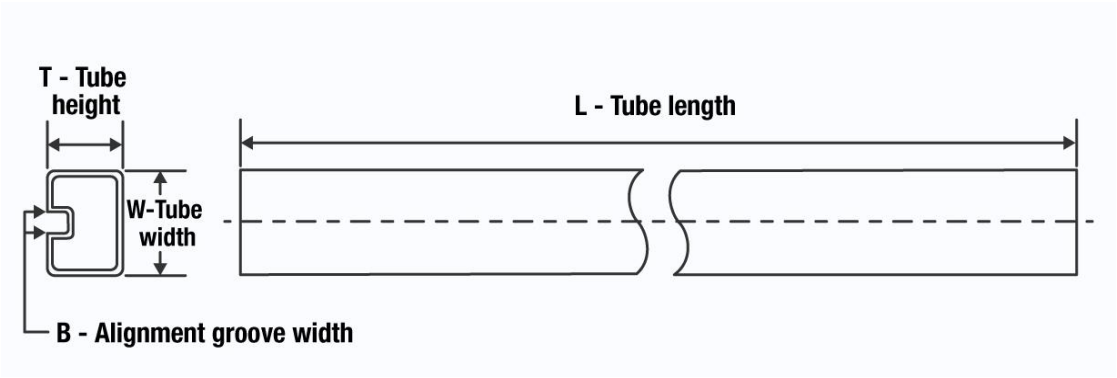
Distribution plot characteristics	price
average slope rate （TL to Tp）	Maximum 3°C/second
preheat Minimum temperature (Ts min) Maximum temperature (Ts max) Time (minimum-maximum) (ts)	 150℃ 200℃ 60-180 seconds
Ts max-TL Inclination rise rate (Ts max to TL)	Maximum 3°C/second
Keep the above time - temperature （TL） - time （tL）	 217℃ 60-150 seconds
Peak temperature (Tp)	260+5/-0℃
Time (tp) within the actual peak temperature of 5°C	20-40 seconds
tilt rate	Maximum 6°C/second
Time from 25°C to peak temperature	Maximum 8 minutes
holding temperature TL peak temperature Tp Average Tilt Rate (TL to Tp)	217℃ 260℃ Maximum 3°C/second

4 Packaging Information

The chip is available in two packaging options: tube and tape, with the specifications as follows.

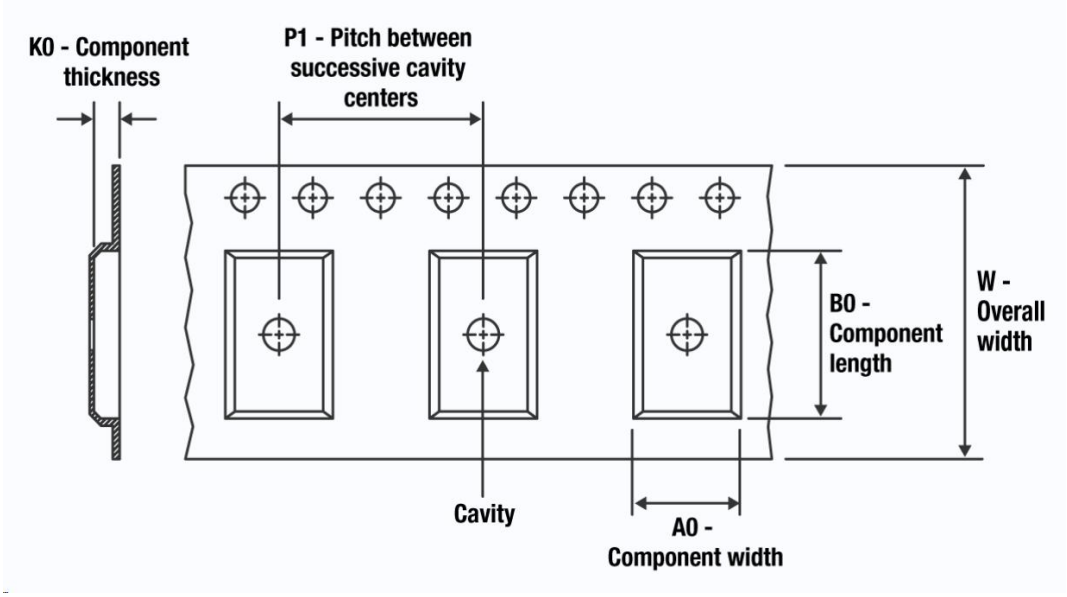
4.1 Material Pipe Specifications

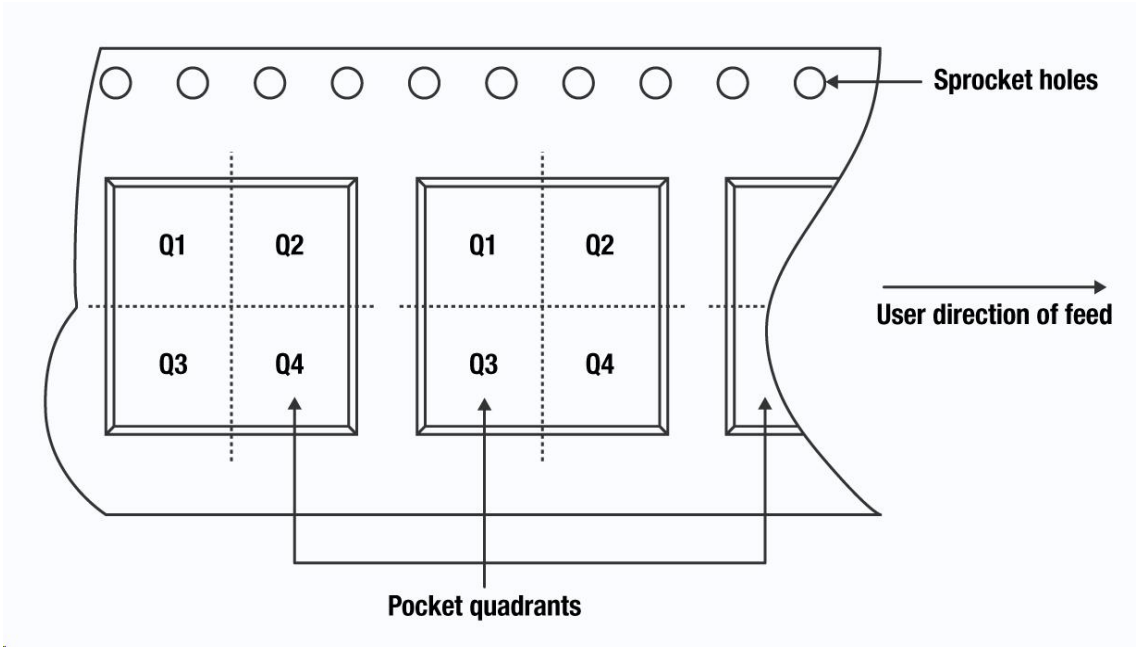
encapsulation form	pipe fitting						
	Quantity per tube	B(mm)	T(mm)	W(mm)	L(mm)	Quantity per box	Quantity per box
SSOP24L	60	5.0±0.15	3.5±0.1	10.8±0.1	520±1.0	10000	60000
SOP16L	50	2.4±0.1	3.4±0.1	7.8±0.1	520±1.0	10000	60000



encapsulation form	braid											
	Quantity per tray	Quantity per box	Spool diameter (mm)	drum width（mm）	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	D0 (mm)	W (mm)	Pin1 quadrant
SOP16L	3000	30000	330±1	16 4±0 2	6 7±0 1	10 4±0 1	2 0±0 1	4 0±0 1	8 0±0 1	1 5+0 1	16 0±0 1	Q1（upper left）
SSOP24L	2000	20000	330±1	16 4±0 2	8 4±0 1	8 7±0 1	2 5±0 1	4 0±0 1	12 0±0 1	1 5+0 1	16 0±0 1	Q1（upper left）

4.2 Tape Specifications




Sprocket holes
Q1
Q2
Q3
Q4
Q1
Q2
Q3
Q4
User direction of feed
Pocket quadrants